The Dissertation Committee for Saungeun Park Certifies that this is the approved version of the following dissertation:

Chemical Vapor Deposited Two-Dimensional Material Based High Frequency Flexible Field-Effect Transistors

Committee:

Deji Akinwande, Supervisor

Sanjay Banerjee

Ananth Dodabalapur

Leonard F. Register

Li Shi

Chemical Vapor Deposited Two-Dimensional Material Based High Frequency Flexible Field-Effect Transistors

by

Saungeun Park

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May 2018

Dedication

This dissertation is dedicated to my parents and brother for their endless love and support.

Acknowledgements

For 5 years at the University of Texas at Austin, I have taken an incredible journey in my life. Everything that I saw, heard and felt at here will be an invaluable nutrient for the remaining life, and I would like to express my sincere gratitude to people around me for their endless support and belief.

First of all, I would like to extend my gratitude to my advisor, Prof. Deji Akinwande. During Ph.D. program at UT Austin, I have been lucky to learn his solid engineering knowledge and attitude, endless passion for research, his standard work ethics. All of experience under his advises shape me into a professional engineer, and it will be proficient for my future careers. I also want to thank my dissertation committee members Prof. Sanjay Banerjee, Prof. Ananth Dodabalapur, Prof. Leonard F. Register, and Prof. Li Shi for providing helpful discussion to my researches. With their Ph.D. students' co-work, I could efficiently extend my research area and perspectives.

I appreciate all the support from my colleagues in the MER building. Dr. Jongho Lee has provided me with a lot of helpful suggestions and skills for my Ph.D. work. I would also express my thanks to our MER members: Dr. Li Tao, Dr. Somayyeh Rahimi, Dr. Alvin Lee, Dr. SK Fahad Chowdhury, Dr. Hsiao-Yu Chang, Dr. Weinan Zhu, Dr. Maruthi Yogeesh, Dr. Shideh Kabiri, Milo Holt, JoonSeok Kim, Wei Li, Ruijing Ge, Md Hasibul Alam, Xintong Li, Myungsoo Kim, Shijiao Han, Xu Jing, and Weiyi Lin. In addition, Atresh Sanne, Amritesh Rai, Hema C.P. Movva, Harry Chou, Jaehyun Ahn, and Dr. Donghyi Koh in Prof. Banerjee group. Dr. Seonpil Jang, Dr. Seohee Kim, and Prof.

Bongjun Kim in Prof. Dodabalapur group. Dr. Mir Mohammad Sadeghi and David Choi in Prof. Li Shi group.

My life at UT Austin has been really wonderful with pleasant and brilliant friends. I thank Narae Yoon, Prof. Jongwon Lee, Kyung Hwan Kim, Jaehyun Kim, Dr. Junggoo Song, Hyoyoung Jeong, Junse Lee, Jaesung Lee, Junmo Sung, Taewoo Ha, Soonil Lee, Yoonho Seo, Sungkyu Kwon, Taehyun Kim, Kyungmin Yoo, and many others. I also want to thank to Melanie Gulick and Melody Singleton for their help.

I want to express my thanks to my best friends, Changmin Lee at UCSB and Joon Sohn at Stranford Univesity. I really appreciate their heartwarming friendship.

Finally, I would like to express my appreciation to my parents, Prof. Byung Tae Park and Sungmi An for their endless encourage and support for my Ph.D. as well as my brother Dr. Sang Uk Park. None of anything I have achieved at UT Austin would have been possible without them.

Chemical Vapor Deposited Two-Dimensional Material Based High Frequency Field-Effect Transistors

Saungeun Park, Ph.D.

The University of Texas at Austin, 2018

Supervisor: Deji Akinwande

Flexible nanoelectronics have attracted great attention due to interesting concepts such as wearable electronics and internet of things, which requires high speed and low power consumption flexible smart system with functions ranging from sensing, computing to wireless communicating. In this dissertation, transparent and solution processable nanoscale polyimide film for highly flexible gate dielectrics is demonstrated by *in-situ* opto-electro-mechanical measurement and utilized for two-dimensional nanomaterials-based field-effect transistors (FETs). Graphene thin film transistor with the nanoscale polyimide dielectric on flexible glass is operated in extremely high frequency regime and shows the highest experimental saturation velocity (~8.4×10^6 cm/s) in any materials in any flexible transistors. Molybdenum disulfide (MoS_2) based transistors with embedded gate structure on rigid substrate are demonstrated with enhancement mode operation, ON/OFF ratio over 10^8, the highest transconductance (~ 70 μS/μm) and saturation velocity (~1.8×10^6 cm/s). CVD MoS_2 FETs on flexible plastic substrates are also demonstrated, showing enhancement mode operation, ON/OFF radio over 10^{10} and transconductance (~6 μS/μm). The flexible CVD MoS_2 transistors with embedded gate structure were employed to study effects of substoichiometric doping by HfO_{2-x}. After the doping layer, the flexible

MoS_2 transistors show ×8 higher source-drain current density as well as more than ×2 mobility improvements. For the another first demonstration, GHz operation and flexibility of graphene and MoS_2 based FETs are realized on commercial available paper substrates, which indicates flexible two-dimensional material based nanoelectronics can be implemented on paper substrates for systems, sensors, and Internet of Things.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction to Two-Dimensional Material Based Flexible Electronics and Applications

Two-dimensional (2D) materials are atomically thin crystalline sheets with a variety of electronic band structures, induced by intralayer covalent bond of neighboring atoms and interlayer van der Waals bonding of layered atomic sheets [1]. Graphene, the planar honeycomb structure composed of carbon, has unique electronic band structure, which conduction band and valence band meets at a point, so called the Dirac points [2]. With the strong carbon-to-carbon intralayer bonding, graphene can be considered as flexible semi-metal nanomaterial. Transition metal dichalcogenide (TMD) nanomaterial, composed of one transition metal atom and two chalcogen atoms with sandwich structure, has direct (indirect) electronics bandgap for the monolayer (for bulk) [3]. Xene, composed of group IVA with buckled hexagonal honeycomb structure, is also 2D semiconducting material with sizable bandgap [4-6]. Hexagonal boron nitride (h-BN), made of boron and nitrogen diatomic planar sheet, has wide bandgap, high thermal and chemical stability [1, 7]. Each van der Waals layered nanomaterial has mechanical flexibility as well as different electronic band structures, such as semi-metal, semiconductor and insulator, it has been intensively studied in the field of flexible/wearable electronics over a decade.

Flexible electronics have attracted great attention due to it interesting concepts such as sensing, computing and wireless communicating, which require low power consumption, high speed operation and mechanical reliability. Thus, many researches on organic, amorphous, and metal oxide FETs have been explored for flexible electronics due to printability of semiconductor material on flexible substrates for massive production [8-

10]. However, its low charge mobility limits GHz operation for wireless communication applications.

Graphene, flexible semi-metal nanomaterial, has been intensively studied due to its outstanding charge transport in the field-effect transistors (FETs); carrier mobility exceeding to 100,000 (10,000) cm^2/Vs for suspended device [11] (for graphene channel on oxide) at room temperature, respectively, which can be utilized for analog, radio frequency (RF), and sub-THz applications. In addition, strain limit of graphene is over 30 %, which is critical factor for flexible/wearable applications [12, 13]. In terms of large production, chemical vapor deposition methods enable to grow wafer-scale graphene [14]. However, due to the lack of bandgap of graphene, graphene transistors have a major drawback for digital logic applications.

Monolayer molybdenum disulfide (MoS_2) is one of TMD materials, which has direct gap semiconductor (~1.8 eV), comparable field mobility (~170 cm^2/Vs) at room temperature [15], and mechanical flexibility [16]. Thus, intensive studies on MoS_2 have been done for the flexible, low power switching and digital logic systems [17-19]. Note that the monolayer MoS_2 is also intensively employed in the field of optoelectronics due to its direct band gap [20].

The charge mobility is one of important device performance parameters, which can be used to determine the cut-off frequency (f_T) at low source-to-drain electric field region as following equation1.1 [1].

$$f_T = \frac{v}{2\pi L} \approx \frac{1}{2\pi}\left[\left(\frac{\mu E_{DS}}{L}\right)^{-1} + \left(\frac{v_{sat}}{L}\right)^{-1}\right]^{-1} \qquad \text{(Equation 1.1)}$$

where L is gate length, E_{DS} is electric field across drain to source, and v_{sat} is saturation velocity.

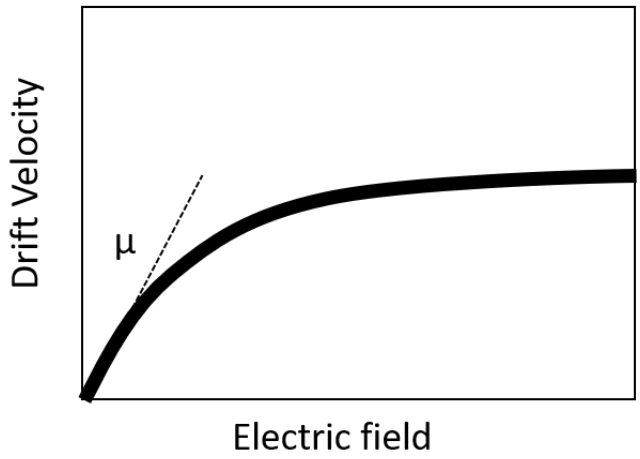

Figure 1.1: Drift velocity as a function of electrical field in a crystal.

As figure 1.1 shows, under the low electric field operation, the former term including carrier mobility dominates, which shows constant slope that is mobility. Also, under high electric field operation, the latter term including saturation velocity dominates. Note that the drift velocity in a crystalline solid at a certain temperature linearly increases with increasing the electric field at low field regime, and the slope is the charge mobility in the crystalline solid. As electric field increases more, the drift velocity doesn't increase linearly due to optical phone scattering, but it saturates to a certain velocity, which is the saturation velocity that is the maximum velocity of a crystalline solid at a certain temperature. The definition of saturation velocity indicates that (i) the highest speed of device is limited by the saturation velocity of the crystal channel material, and (ii) high electric field is required to operate transistors in saturation velocity regime.

Another important parameter for high speed operation of transistors is contact resistance [21-23]. Especially, voltage drop across contacts at source and drain leads to decreased intrinsic S/D voltage that applied to active channel, followed by degradation of transconductance. The transconductance is proportional to important RF metric ($f_{T,int}$·L), contact resistance engineering has been actively investigated [1]. In this section, contact resistance dependent on three device structures will be studied in terms of RF performance. The embedded gate structure, which is gate first process, has been proposed due to (i) high-k dielectric scalability without seed layer, (ii) reduced number of process steps after CVD 2D layer transfer, and (iii) residue-free 2D layer and gate dielectric interface [24-26]. The detailed advantages of embedded gate structure will be introduced in following sessions.

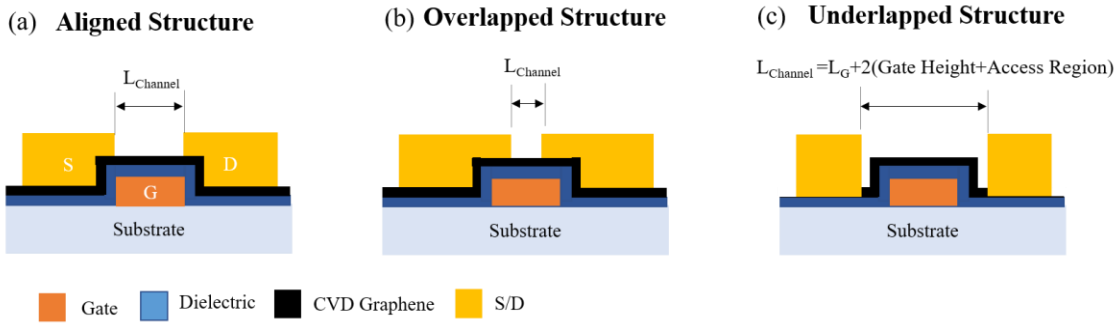

Figure 1.2: Embedded gate with three different structures. (a) aligned structure. The channel length ($L_{Channel}$) is same as the gate length. (b)overlapped structure. $L_{Channel}$ is shorter than the gate length, which has large gate and S/D overlapped area. (c)underlapped structure. $L_{channel}$ is same as 2·(gate height+access region), which is longer than the gate length.

The embedded gate structure has three different types: aligned, overlapped and underlapped source and drain structure as shown in Figure 1.2. Figure 1.2(a) shows the aligned gate and S/D structure that the channel length is same as the gate length, and

channel length of overlapped (Figure 1.2(b)) and underlapped (Figure 1.2(c)) structures is defined by the gap between S/D and the gate length (gate length + 2×(gate height+ungated region)), respectively. Note that the gate height is the gate metal thickness, and the access region is the ungated channel length. In terms of parasitic capacitance between gate and S/D, the underlapped structure has the air dielectric (dielectric constant is 1) at the middle of gate and S/D, so the underlapped structure is highly desired to reduce parasitic capacitance effects, resulting higher extrinsic cut-off frequency performances. The parasitic capacitance of overlapped structure more severe, and the amount of extrinsic RF performance degradation is proportional to the channel width that is usually large width for RF FETs. However, the overlapped structure enables to reduce contact resistances due to gate field assisted doping at contact, resulting improved transconductance. The reduced contact resistance is critical to improve transconductance (Equation 1.2) [27, 28].

$$g_m = \frac{G_m}{1-G_m[R_s+(R_s+R_d)/(G_m/G_{ds})]} \qquad \text{(Equation 1.2)}$$

where G_m is extrinsic transconductance, R_s is contact resistance at source side, R_d is drain contact resistance, and G_{ds} is the extrinsic device conductance (dI_d/dV_d).

In order to improve contact resistance, understanding of charge injection mechanism is required.

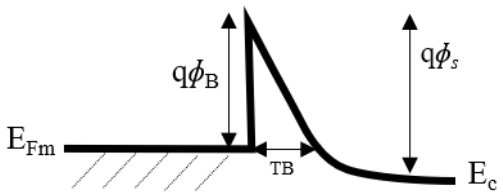

Figure 1.3: Band diagram of the interface between metal and n-type semiconductor under surface potential, inducing band bending of conduction band downward. ϕ_B is SBH, ϕ_s is the surface potential, E_{fm} is the metal work function energy, E_c is conduction band energy of n-type semiconductor, and TB is the tunnel barrier.

Figure 1.3 represent a band diagram of metal-n-type semiconductor interface under surface potential, where ϕ_B is SBH, ϕ_s is the surface potential, E_{fm} is the metal work function energy, E_c is conduction band energy of n-type semiconductor, and TB is the tunnel barrier.

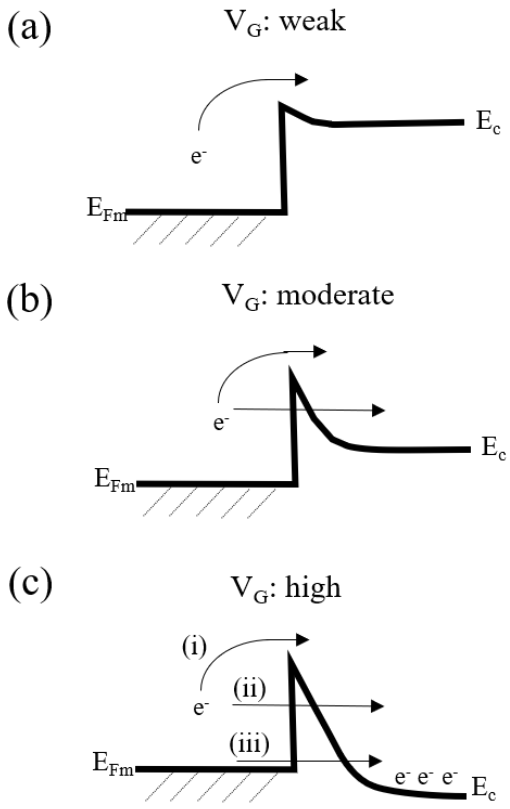

Figure 1.4: Three mechanisms of charge injection at the contact: (i) thermionic injected emission, (ii)thermionic-field emission, and (iii) field emission. (a) band diagram of metal-semiconductor contact under weak gate bias. Charge carriers thermally overcome the Schottky barrier for charge injection. (b) band diagram of metal-semiconductor contact under moderate gate bias. Both thermionic emission and thermionic-field emission contributes to the charge injection. (c) band diagram of metal-semiconductor contact under strong gate voltage. Three charge injection mechanisms, including thermionic, thermionic-field, and field emission, contribute to the contact resistance.

Figure 1.4 shows three charge injection mechanisms such as (i) thermionic emission, (ii) thermionic-field emission, and (iii) field emission. Figure 1.4(a) shows under weak surface potential, which allow thermionic carrier injection over Schottky barrier. The

thermionic emission current at metal-semiconductor interface can be explained by the thermionic emission diffusion theory, and the equation 1.3 is shown in below.

$$J_{thermionic} = \mathrm{A} \cdot T^{\alpha} \cdot exp^{-\frac{q\Phi_B}{k_B T}}[1 - exp^{-\frac{qV}{k_B T}}] \qquad \text{(Equation 1.3)}$$

where A is the Richardson constant, T is the temperature, α is a constant equal to 2 for bulk semiconductors and 3/2 for two-dimensional semiconductor [23], and ϕ_B is the SBH, k_B is the Bolzmann constant, and V is applied voltage to metal-semiconductor junction. When $k_BT \ll qV$, the equation 1.3 can be simplified to equation 1.4

$$J_{thermionic} = \mathrm{A} \cdot T^{\alpha} \cdot exp^{-\frac{q\Phi_B}{k_B T}} \qquad \text{(Equation 1.4)}$$

According to the equation 1.4, thermionic charge injection depends on Schottky barrier height (SBH) and temperature, and the thermionic charge injection happens at both low and high gate voltage doping on semiconductor. At high gate voltage, tunnel barrier at metal-semiconductor interface get thinner, and the mechanism of the thermionic field emission current starts, which is the Fowler-Nordheim (FN) tunneling. The FN tunneling assisted current is proportional to V^2, where V is the applied voltage at the interface. Therefore, the thermionic field emission usually starts at high S/D voltage. When the gate voltage is high enough to induce band bending of conduction band of n-type semiconductor below the work function energy of S/D metal as well as the thin tunnel barrier, field emission injection (direct tunneling) starts at high gate and S/D voltage as shown in Figure 1.4(c).

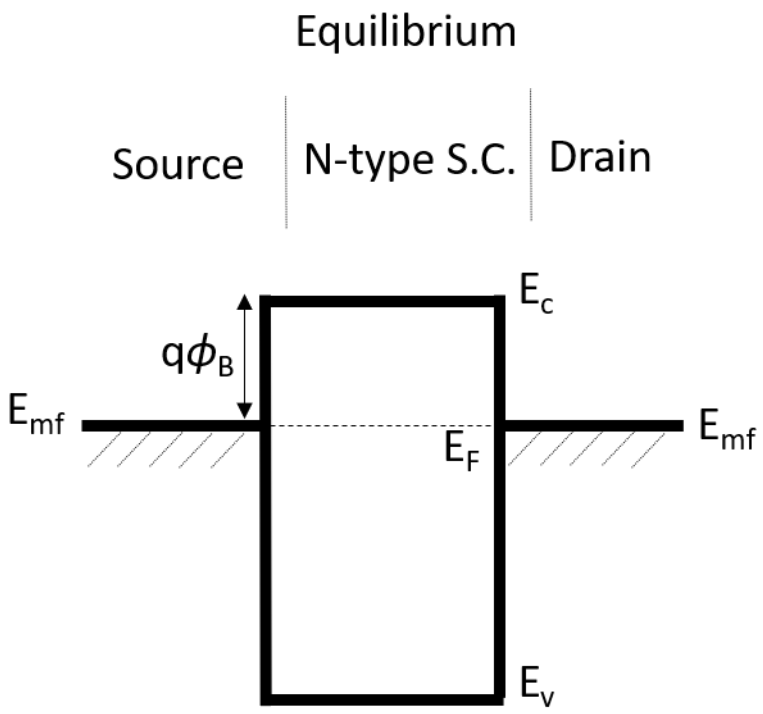

Figure 1.5: Band diagram of metal-semiconductor contacts at equilibrium. The ϕ_B is barrier height (V), and E_v and E_c is energy of valence band and conduction band, respectively. E_{mf} is work function energy (eV) for S/D metal. E_f is the fermi energy that is pinned to metal contact's work function energy.

Figure 1.5 represents band diagrams through source to drain and MoS_2 n-type semiconductor at the equilibrium, which there are no gate and S/D bias. ϕ_B is barrier height (V), and E_v and E_c is energy of valence band and conduction band, respectively. E_{mf} is work function energy (eV) for S/D metal. The work function energy of S/D is pinned to fermi energy of MoS_2 due to two interface behaviors such as metal work-function modification by interface dipole formation due to charge redistribution as well as production of gap states mainly due to weakened intralayer S-Mo boding [23, 29].

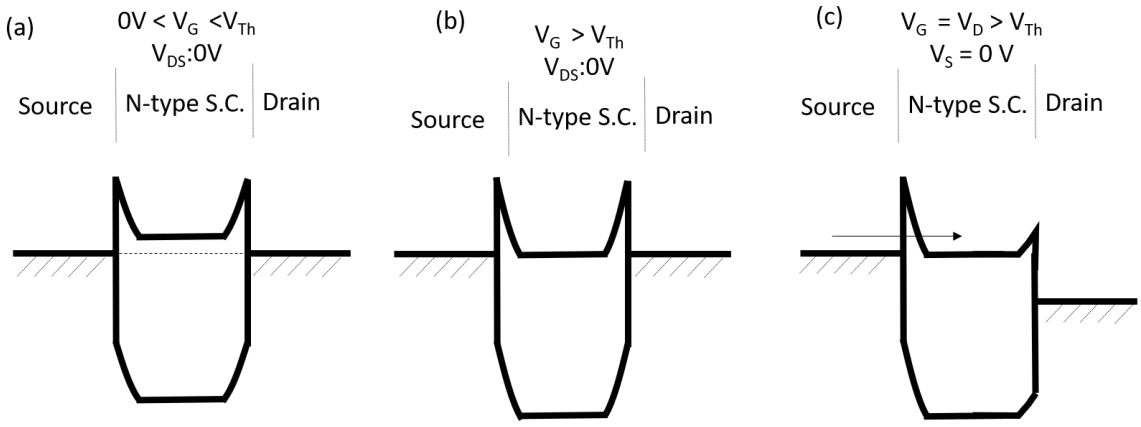

Figure 1.6: Band diagram of S/D contacts under bias conditions. (a) under positive gate bias (V_G) less than threshold voltage (V_{Th}). (b) under positive V_G over V_{Th} and no V_{DS} voltage. (c) V_G and drain bias (V_D) is over V_{Th} while V_S = 0V. Note that Schottky barrier height is independent on the external applied bias.

Band diagram of S/D contacts and n-type semiconductor under bias condition are shown in Figure 1.6(a), (b), and (c), which shows basic qualitative insight for charge transport at contact. When positive voltage (<V_{Th}) is applied to gate, corresponding surface potential induce n-type semiconductor band bending downward, forming thin tunnel barrier. Under the drain bias that is same as gate voltage, the band bending at drain side is moved downward, leading to drain electrons (Figure 1.6(c)). Note that the barrier height (Schottky barrier) is independent on external voltage and it depends on material properties, such as doping concentration of semiconductor and S/D metal work function. Both Schottky barrier and tunnel barrier mainly impede the charge injection at contact resulting in degradation of I-V characteristics.

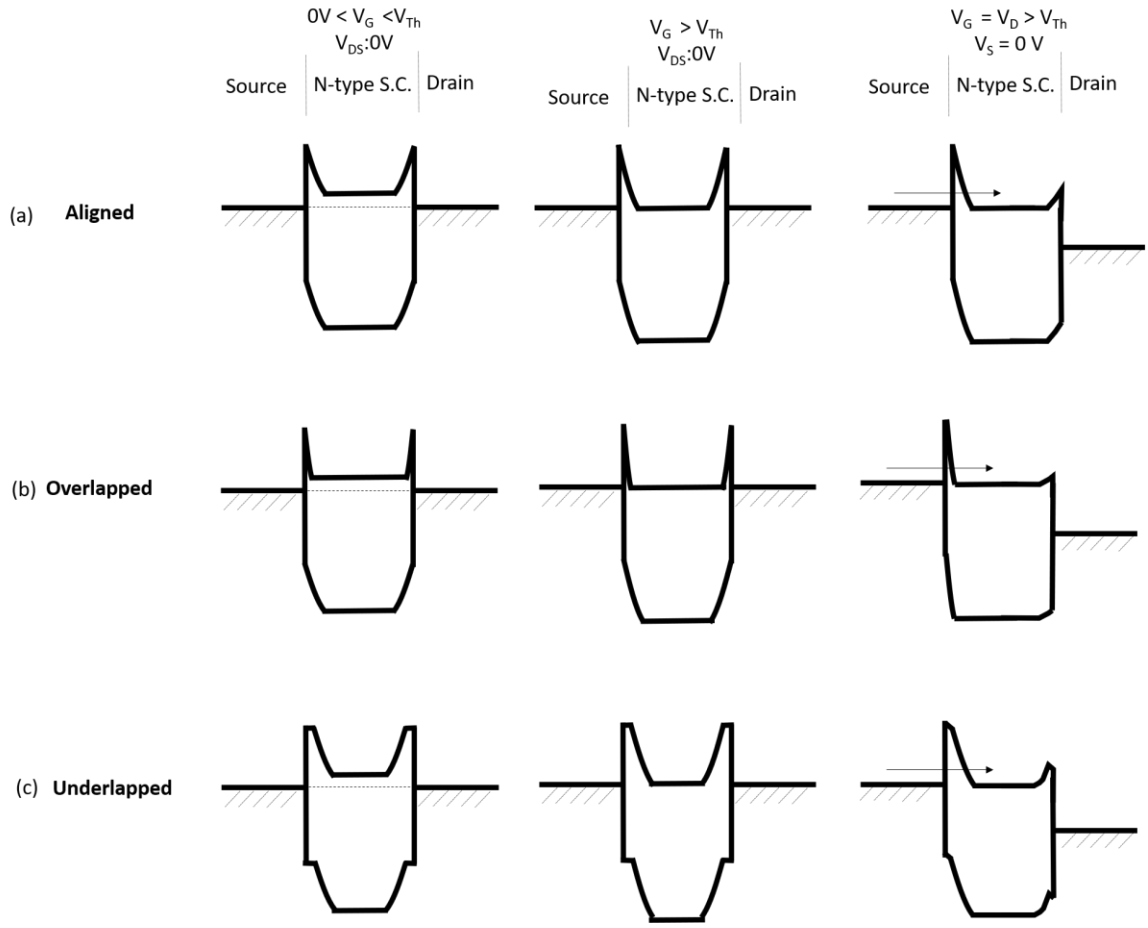

Figure 1.7: Bias condition dependent band diagrams for three different device structures, such as (a) aligned, (b) overlapped, and (c) underlapped structure, under different applied voltage conditions (V_G and V_D).

Figure 1.7 represents band diagrams for three different device structures under different conditions of applied voltage. In the case of overlapped structure (Figure 1.7(b)), the tunnel barrier is shorter than the one of aligned structure due to the gate-field-assisted short tunnel barrier. Under the gate bias condition, the electrical field between gate and S/D induces charge carriers in 2D semiconductor layer, making tunnel barrier be thinner. Note that there is no gate field induced charge carrier at contact in the top-gated structure

due to screening effects. In the case of the underlapped structure, however, there is two access regions at the side of S/D, which cannot be field-assisted doped, resulting in long tunnel barrier for the charge transport and higher contact resistance (Figure 1.7(c)). Thus, although underlapped structure is beneficial to achieve higher extrinsic RF performance, it shows worse DC characteristics due to the existence of tunnel barriers, such as Schottky characteristic in output characteristic. Note that small bandgap semiconducting materials, such as black phosphorus (0.3 eV), usually present the inversion layer near the contact interface at relatively lower surface potential. Thus, if we assume same SBH for large and small bandgap semiconductor, small bandgap material shows more band bending, corresponding to the better charge injection at the same surface potential.

Chapter 2: Flexible Gate Dielectric: Nanoscale Polyimide

Flexible electronics with mechanically strong compliant materials, such as 2D semiconducting nanomaterials, has attracted research attention for a wide variety of device applications such as foldable, bendable and stretchable communication systems, sensors and displays [1, 5, 18, 26, 30-34]. In order to fulfill the full potential of 2D semiconductors for flexible thin-film transistors (TFTs), high strain durable, electrically stable and smooth gate dielectric films are required [1, 26, 32, 33]. Despite the importance of mechanical flexibility of gate dielectric, there have been rather limited studies examining practical flexible gate dielectric systems. Thus far, metal oxide dielectric films such as Al_2O_3 and HfO_2, which can afford high dielectric constants and are readily deposited by atomic layer deposition (ALD), have been widely utilized to improve transistor electrostatic gate control while providing conformal coverage [18, 26, 35, 36]. However, commonly used high-κ and inorganic dielectrics are rigid with low mechanical flexibility limited to around 2 % tensile strain with subsequent mechanical cracking which can lead to current leakage path as the failure mechanism at high strains [18, 37, 38].

The results described in this chapter have been published in: "Transparent Nanoscale Polyimide Gate Dielectric for Highly Flexible Electronics," Advanced Electronic Materials, Vol. 4, issue 2, 2018, by S. Park, H.-Y. Chang, S. Rahimi, A. L. Lee, L. Tao and D. Akinwande (Reused with permission from John Wiley and Sons with license number, 4336580809874). Contribution: S. Park contributes to synthesis and curing recipes of nanoscale polyimide, electro-mechanical measurements, optical characterization with UV-vis, and graphene device fabrication. H.-Y. Chang helped to optimize the curing temperature of nanoscale polyimide dielectric, FTIR measurements, and MoS_2 device fabrication and electrical measurements. S. Rahimi, A. L. Lee, and L. Tao contributed to improve CVD graphene quality with helpful discussion, and D. Akinwande supervised all of works, and all authors reviewed and commented on the results and manuscript. D. Akinwande is the corresponding author for the publication.

The work by Liu et al. proposed vapor phase self-assembled nanodielectric (v-SAND) as a gate dielectric due to its outstanding electrical, optical properties and compatibility to most plastic substrates [39]. However, performances of organic TFTs using v-SAND degrade during bending because of gate leakage current. On the other hand, several polymeric dielectrics have shown significantly outstanding mechanical flexibility, but operation voltage is usually quite large due to the relatively thick films needed to ensure low gate leakage current [8, 9, 40, 41]. Polyimide, among many polymeric dielectrics, has been widely studied as a gate insulator for flexible organic electronics due to its high chemical stability and good insulation properties [9, 40, 42]. However, it also requires the large operating voltage due to its thickness (typically approaching micrometer thickness). As such, research is warranted on realizing nanoscale (≤100 nm-thick) insulating advanced materials that can be used as gate dielectrics for highly flexible TFTs and systems that can substantially exceed the 2 % strain limitation of metal oxide films.

In this chapter, we report the transparent and solution-processable nanoscale polyimide (NPI) films less than 100 nm-thick and its applications as flexible gate dielectrics for 2D materials-based transistor devices. Stable electrical performances of NPI dielectric under high tensile strains up to 10 % are demonstrated by in-situ bending experiment [43, 44]. A welcome benefit of the NPI nanoscale thickness is that the optical transparency is improved over 84 % across the visible spectrum compared to conventional thick polyimide, indicating suitability for transparent electronics, such as display and sensor. Prototypical 2D active materials, molybdenum disulfide (MoS_2) and graphene

using NPI gate dielectric show outstanding TFT properties comparable to performances of similar devices using ALD gate dielectrics. For instance, MoS_2 FETs with NPI dielectric affords maximum field-effect mobility of 30 $cm^2/V{\cdot}s$ and ON/OFF current ratio $>10^7$. Graphene FETs (GFETs), fabricated with NPI dielectric, also show DC and radio frequency (RF) performances comparable to similar devices with high-κ dielectrics, such as maximum carrier mobility of ~ 5170 $cm^2/V{\cdot}s$ [26, 31]. An extrinsic cutoff frequency ~6.5 GHz is achieved, which reveals that NPI is also a suitable dielectric for flexible RF TFTs for wireless communication systems unlike similarly highly flexible ion-gel dielectrics that are limited to kHz frequencies or below [45].

PREPARATION OF NANOSCALE POLYIMIDE FILM

Solution processable nanoscale polyimide (NPI) precursor was obtained through the chemical dilution of liquid polyimide (LPI) precursor (from HD MicroSystems) with N-Methyl-2-pyrrolidone (NMP) (from Sigma-Aldrich) [9, 42]. The thickness of NPI can be controlled by the spin-coating speed as well as by controlling the viscosities obtained by different volume ratio mixing of LPI and NMP [42]. Table 2.1 shows various NPI dielectric thickness with different spin-coating speed and dilution volume ratio [43, 44]. A curing process at 250 °C under nitrogen (N_2) atmosphere for 2 hours was developed to polymerize the solution-based precursor as well as to drive out the remaining solvent. The temperature profile of the curing process is shown in Figure 2.1. The cure heating cycle is required to imidize the nanoscale polyimide precursor converting it to a thin polyimide film and driving out remaining solvents. Temperature increases from room temperature to

200 °C with 4 °C/min of temperature ramping rate. It stays at 200 °C for 30 mins to activate adhesion promoter in liquid polyimide precursor, then oven heats to 250 °C with ramp rate 2.5 °C/min. Temperature holds at 250 °C for 2 hours, and temperature gradually decreases to room temperature.

Spin speed / Volume ratio	3000 rpm	6000 rpm
1:2	191 nm	119 nm
1:3	91 nm	60 nm
1:4	81 nm	51 nm
1:5	50 nm	34.5 nm

Table 2.1: Wide range of NPI dielectric thickness from different spin-coating speed and dilution volume ratio.

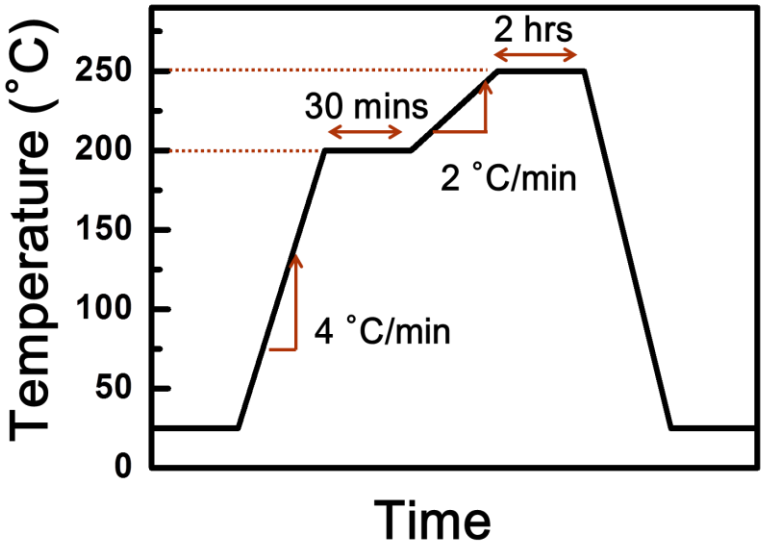

Figure 2.1: Curing process temperature profile for nanoscale polyimide dielectric

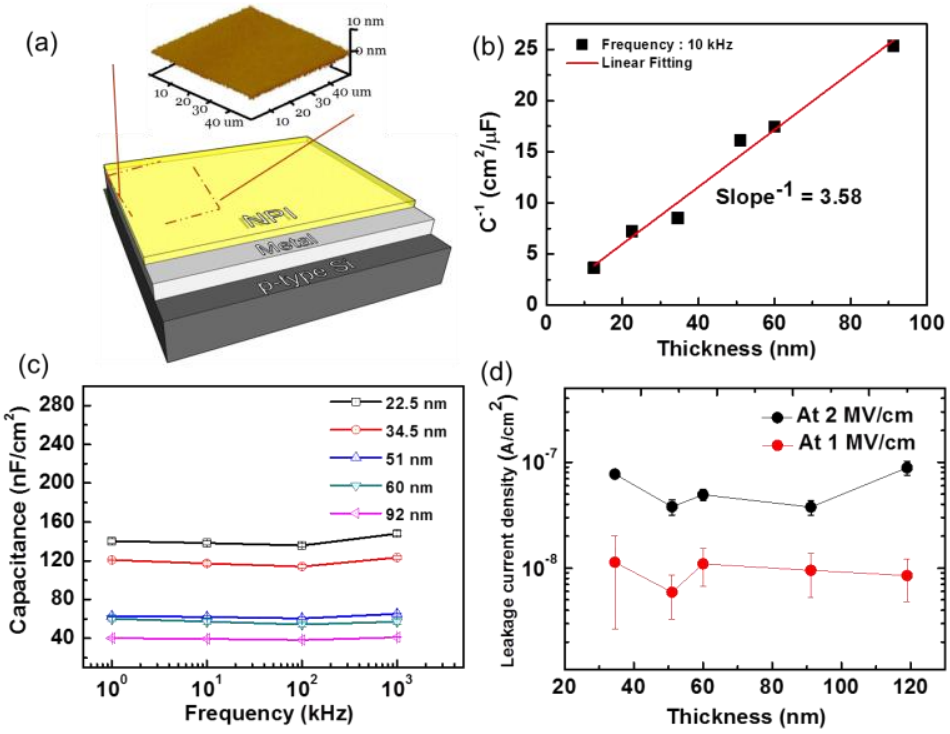

Figure 2.2: Physical and electrical characterization of nanoscale polyimide thin films. (a) NPI surface roughness after curing process on the nickel metal. RMS roughness is less than 0.5 nm for 50 μm × 50 μm area. (b) inverse capacitance as a function of thickness with extracted dielectric constant (~3.58 ± 0.24) of NPI. (c) capacitance as a function of frequency and thickness. All capacitance values are fairly constant in the wide range of frequency (1 kHz to 1 MHz). (d) leakage current density as a function of thickness at 1 MV/cm and 2 MV/cm. Low leakage current density of several film thicknesses at high fields imply the negligible degradation of nanoscale polyimide dielectric after it is properly diluted by NMP.

Figure 2(a) shows the surface topography of NPI on the Ni coated highly doped Si substrate after the curing process, and the corresponding root mean square (RMS) roughness is about 0.5 nm over 50 μm × 50 μm area. It should be noted that the NPI dielectric flattens the rough surface of Ni. The RMS roughness of Ni surface was 0.75 nm

before NPI dielectric formation. The dielectric constant, κ, is extracted from metal-insulator-metal (MIM) test structures fabricated from metal/NPI/highly doped Si, and is determined to be 3.58 ± 0.2 as shown in Figure 2.2(b). Note that the y-intercept of Figure 2.2(b) is the interface capacitance which might be due to the native oxide on Si as well as interface traps [46]. Figure 2.2(c) represents capacitances (up to 140 nF/cm^2) for different NPI dielectric thicknesses. Figure 2.2(d) shows the leakage current densities at the electric field of 1 MV/cm and 2 MV/cm with varying thickness. The relatively flat profile with thickness indicates the well-controlled thickness and negligible degradation of electrical characteristics of nanoscale polyimide, and outstanding leakage current density compared with other flexible dielectrics (Table 2.2).

ELECTRO-MECHANICAL CHARACTERISTICS

In-situ bending measurement were conducted using MIM test structures on Kapton substrate in order to systematically study the electrical performance of NPI dielectric under bending strains as illustrated in Figure 2.3(a).

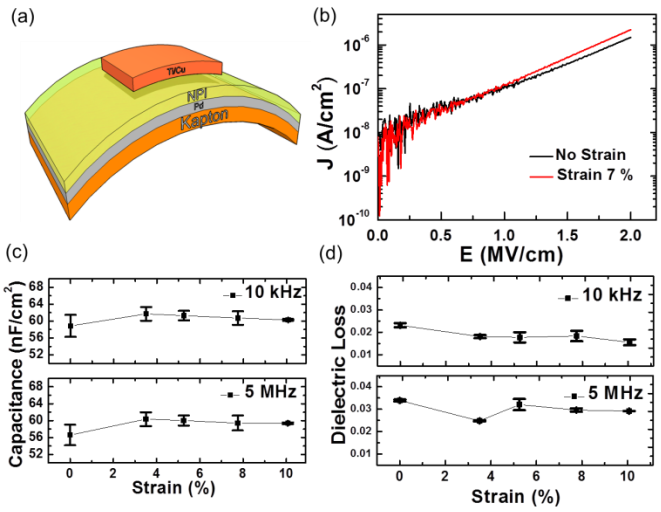

Figure 2.3: Mechanical performance of nanoscale polyimide dielectric. (a) device schematic for the in-situ evaluation for electrical stability under mechanical bending. (b) leakage current density as a function of the electric field under flat and 7 % tensile strain for 60 nm NPI. The leakage current density of flexible MIM devices is an order higher than the leakage current of Si based MIM structure (Figure 2.2(d)). (c), (d) capacitance and dielectric loss as a function of strain up to 10 % for 60 nm NPI, respectively. The consistent performance under large bending conditions affords a realistic prospect for advanced (high-strain) flexible electronics.

NPI solution was spin-coated on Pd/Kapton followed by curing at 250 °C for 2 hours under N_2. Metal contacts (1nm Ti/100 nm Cu) were deposited as a top electrode to complete the device fabrication. The sample with 60 nm NPI was loaded on the in-situ bending fixture as shown in Figure 2.4(a). Optical images of flexible MIM devices under strain up to 10 % are shown in Figure 2.4(b), (c), (d). MIM devices atop surface, which can be seen by optical microscope, were characterized using a semiconductor device parameter analyzer (Agilent B1500A) for current-voltage (I-V) and capacitance-voltage (C-V) characteristics. Figure 2.3(b) details the leakage current density as a function of

electric fields under flat and 7 % tensile strain conditions. Notably, the leakage current density at 7 % strain is comparable with that of previously reported flexible dielectrics, such as high-κ dielectric and v-SAND dielectric, without strain [10, 39, 47, 48]. Note that the leakage current density of flexible MIM devices is an order higher than the leakage current of Si based MIM structure (Figure 2.2(d)). We attribute this to the locally enhanced electrical field induced by rough surface of polyimide substrate. Figure 2.3(c) and 2.3(d) are the C-V characteristics of NPI at 10 kHz and 5 MHz, where the maximum measurement frequency is limited by the measurement setup. The capacitance variation under up to 10 % strain is very small as shown in Figure 2.3(c). In addition, dielectric loss less than 0.04 is measured at strain up to 10 % (Figure 2.3(d)), suggesting that dielectric relaxation is negligible.

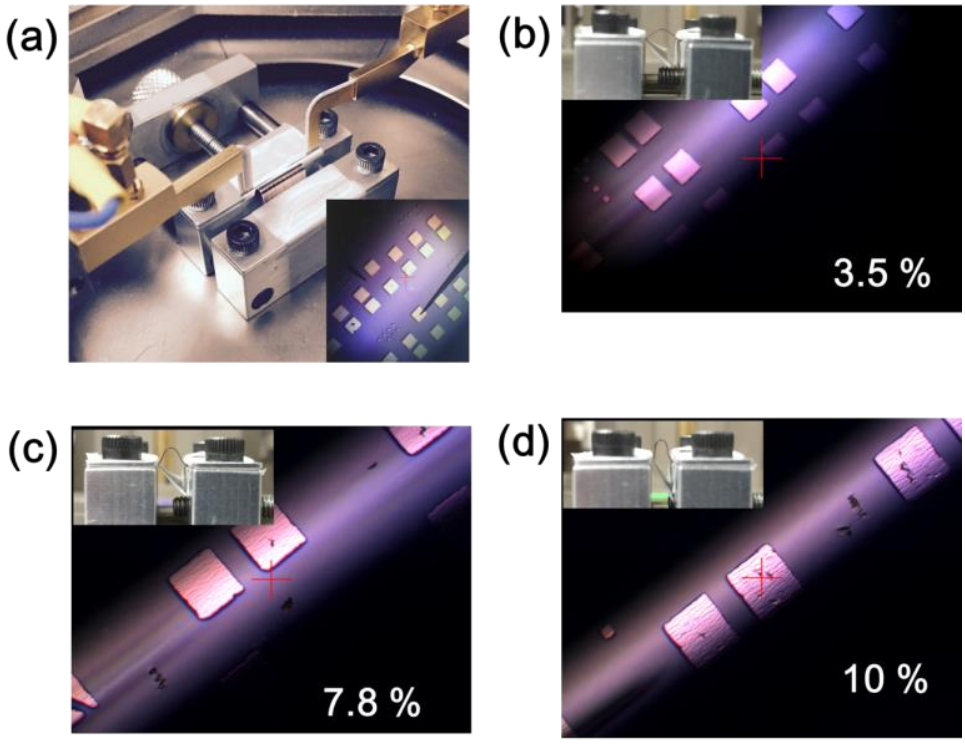

Figure 2.4: In-situ electro-mechanical measurement. (a) an image of an electrical measurement system with a flexible MIM sample under 10 % tensile strain. Inset shows an optical image of flexible MIM devices during in-situ bending test. (b, c, d) optical images for flexible MIM device under strain up to 10 %. For accurate in-situ electromechanical measurement, atop surface devices, which can be seen by optical microscope, were characterized. Insets show each side-view of bent substrate in a strain apparatus.

Table 2.2 shows a comparison of some dielectric properties for various flexible dielectrics that have been reported. Note that this work is the first practical study for in-situ electro-mechanical measurement with up to 10 % strain, but other studies on flexible dielectric were done with the ex-situ measurement with relatively low strain (measurements were mostly done on flat sample after applying low strain). The stable

electrical performances at large bending conditions demonstrate that NPI is a promising flexible dielectric compared to existing alternatives.

	Thickness [nm]	RMS Roughness [nm]	Dielectric Constant	Dielectric Loss	Leakage Current Density [A/cm^2]	Transparency [%]	Strain/Bending Radius [%/mm]
Al_2O_3 [18]	25	< 1	7	NR	NR	NR	2/2.5
Solution-grown amorphous alumina (Al_2O_x) [49]	93	0.78	9.5	NR	NR	> 76	NR/10
Mylar [41]	2500	0.7	3.25 @ 1kHz 3 @ 1MHz	0.005 @ 1kHz 0.005 @ 1MHz	NR	NR	1/0.2
Inorganic/organic hybrid dielectric (v-SAND) [39]	20	0.84	4.5 @ 1kHz 2.25 @ 1MHz	NR	10^{-6} @1MV/cm	~ 70	0.56/20
Graphene interlayer [50]	1740	NR	52 @ 1kHz 10 @1MHz	0.05 @ 1kHz > 1 @ 1MHz	10^{3} @1MV/cm	> 88	0.83/7.5
This work	60	< 1	3.58 @ 10 kHz	0.03 @ 1MHz	10^{-8} 1MV/cm	> 84	10/0.75

Table 2.2: Comparison of several candidates for the thin-film gate dielectric for flexible electronics

OPTICAL CHARACTERISTICS

Figure 2.5(a) shows the carbonyl region of the FTIR spectrum of polyimide. Similar to the 15 μm-thick PI on the Kapton film, 60 nm-thick NPI on glass had the same characteristic vibration bands near 1778 and 1720 cm^{-1} [51], which are in carbonyl stretching region of the infrared spectra (1600 to 1800 cm^{-1}). The result is consistent with our expectation since the diluting process is not expected to change the chemical composition of polyimide. The optical transparency of 60 nm NPI is shown in Figure 2.5(b), revealing improved transparency over 84 % across the visible spectrum, but the 15 μm-thick polyimide is completely opaque at wavelengths below 400 nm due to light absorption in thick PI dielectric.

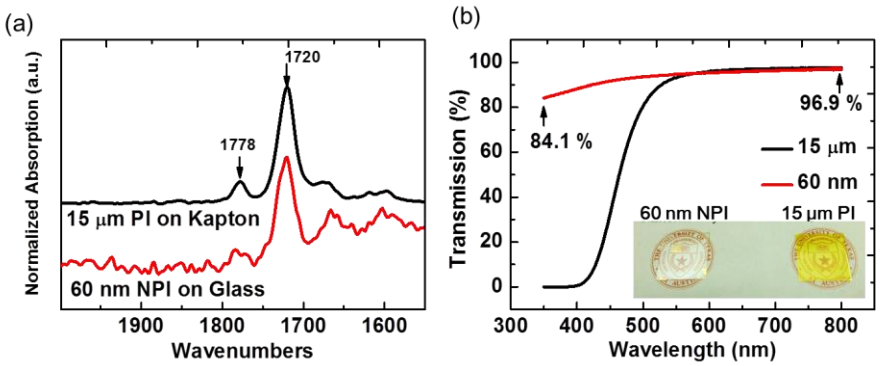

Figure 2.5: Optical studies of nanoscale polyimide. (a) carbonyl region of the FTIR spectrum of 60 nm NPI on glass and 15 μm-thick spin-coated and cured PI on thick Kapton film. Both showed the same characteristic vibration bands near 1778 and 1720 cm^{-1}. (b) optical transparency for PI with thickness of 60 nm and 15 μm on glass substrates. The transparency has improved to more than 84 % for NPI for the entire visible spectrum.

Dependence of optical transmission on the wavelength and the NPI dielectric thickness with different wavelengths is shown in Figure 2.6(a) and (b), which reveals that the transmittance of NPI dielectric increases with decreasing NPI thickness according to the Beer-Lambert law (Equation 2.1):

$$T = e^{-\alpha \cdot d} \qquad \text{(Equation 2.1)}$$

Where T is the transmittance; α is the absorption coefficient; d is the film thickness (path length). The exponential dependence of transmittance on the NPI thickness for low wavelength range (300 to 450 nm) are shown in Figure 2.6(c), (d), and (e), and extracted absorption coefficients for the wavelength region are 2500 ± 320 (for 400 nm wavelength), 25700 ± 4700 (for 350 nm wavelength), and 108000 ± 14700 (for 300 nm wavelength). The outstanding optical transparency indicates that the NPI film is a suitable candidate for the dielectric for TFTs which requires transparency, encapsulation for solar cells, and orientation films in liquid crystal display devices (LCDs).

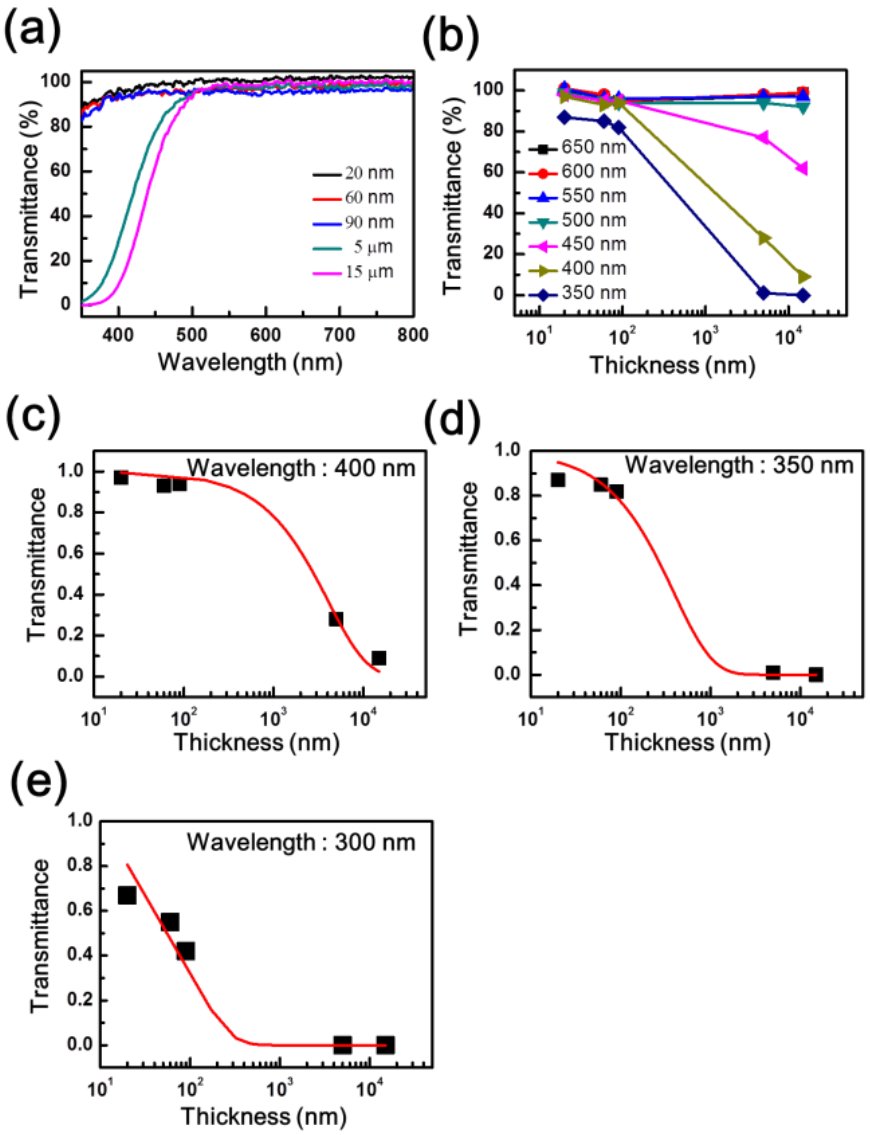

Figure 2.6: Dependence of NPI optical transmission on (a) wavelength and (b) NPI thickness. Dependence of NPI optical transmission for wavelength, (c) 400 nm, (d) 350 nm, (e) 300 nm, on thickness. The exponentially decaying transmittance as a function of thickness shows NPI dielectric well follows the Beer-Lambert law, $T = e^{-\alpha \cdot d}$, where T is the transmittance; α is the absorption coefficient; d is the film thickness.

TWO-DIMENSIONAL MATERIAL TRANSISTORS WITH NANOSCALE POLYIMIDE

For benchmarking the performance of NPI gate dielectrics, TFTs based on MoS_2 and graphene were fabricated. MoS_2, was prepared by mechanical exfoliation of commercial crystals (from SPI supplies) on highly doped Si substrate which is used as the back gate, and 60 nm-thick NPI was spin coated and cured. With this gate stack, the exfoliated MoS_2 flakes with different thicknesses can yield good contrast under optical microscope. Flakes with thickness between 5-20 nm were selected and confirmed by atomic force microscopy (AFM). Source/drain contacts were defined by electron beam lithography (EBL) and lift-off process of 50 nm Au. A schematic of the back-gated MoS_2 device is shown in Figure 7(a). Devices were patterned with a fixed channel length (1 μm) and had varying channel widths (0.5 – 3 μm) that is naturally defined by the width of the exfoliated flakes.

Electrical characteristics of the MoS_2 FETs were then evaluated under ambient conditions. Representative transfer (I_D-V_G) characteristics are shown in Figure 2.7(b). An on/off current ratio of $>10^7$ and a subthreshold swing of ~450 mV/dec were observed. Linear transport at low-fields and current saturation characteristics at high-fields can be seen in the output characteristics (Figure 2.7 (c)). The field-effect mobility is in the range of 8~30$cm^2/V{\cdot}s$ for a variety of devices with the same channel length [52]. Importantly, the exfoliated MoS_2 flakes with NPI gate dielectrics show comparable device performance to the back-gated devices fabricated with SiO_2 or high-κ dielectric with the same device structure and fabrication process [18]. As shown in Figure 7(d), from the statistics of the

mobility extracted from devices with different dielectrics, including SiO_2, high-κ dielectric (Al_2O_3), and NPI (this study), NPI shows comparable mobility to conventional dielectrics in Si fabrication process. This comparative study suggests that NPI is a promising candidate to replace the conventional rigid inorganic dielectrics for highly flexible electronics.

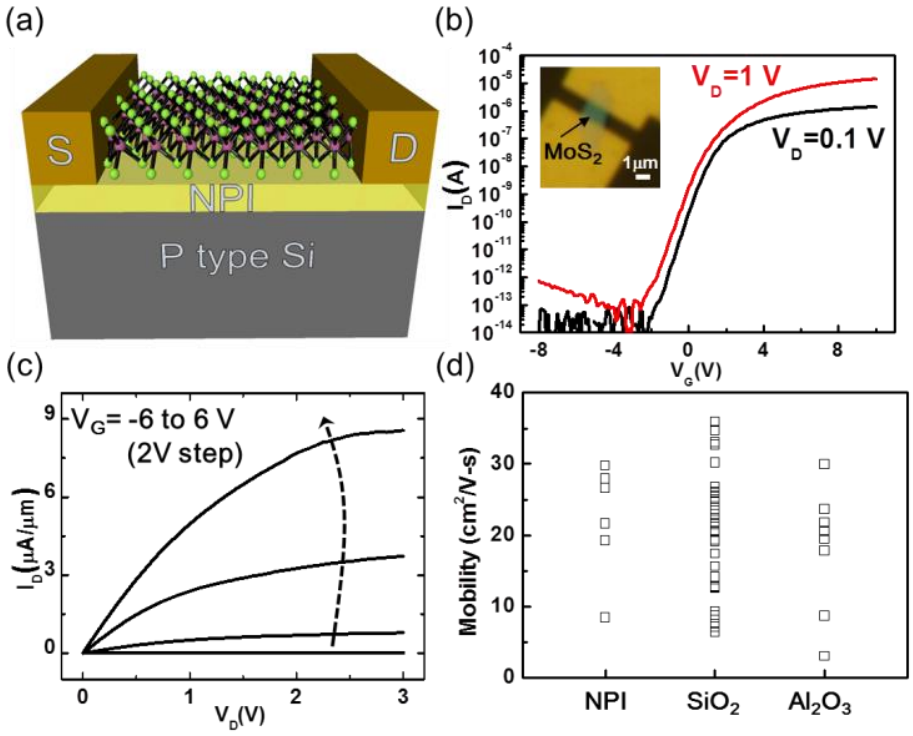

Figure 2.7: 2D semiconductor (MoS_2) TFT with nanoscale polyimide gate dielectric. (a) schematic depiction of the bottom-gate device. (b) transfer characteristics of MoS_2 FETs with 60 nm-thick NPI dielectric. On/Off ratio is larger than 10^7. MoS_2, which is indicated in the insert is ~12 nm-thick with channel dimensions corresponding to L=1 μm and W=1.6 μm. (c) output characteristics show linear transport at low-fields and current saturation at high-fields. (d) comparison of the field effect mobility from several samples using NPI, SiO_2 and Al_2O_3 as gate dielectrics. NPI shows comparable mobility to conventional dielectrics in Si fabrication process.

The fabrication of graphene FETs starts from 300 °C curing process of LPI on PI substrate (~ 127 μm thick) in order to achieve the RMS roughness less than 1nm as described in prior works [26, 31, 32]. The first EBL patterned a gate array that has embedded gate with 6 fingers to enhance the current drive; metal contacts (2nm Ti/38nm Pd) was deposited for embedded gate electrodes. NPI was spin-coated and cured at 250 °C for 2 hours, which formed 60 nm of flexible gate dielectric. Gate pad area was opened by the second EBL and CF_4/Ar Plasma etching. Monolayer graphene grown on copper foil by chemical vapor deposition was then transferred on the patterned device via poly(methyl methacrylate) (PMMA) assisted wet transfer process using ammonia persulfate to etch copper film [14]. The third EBL and O_2 plasma were employed to define the active graphene channel. 250 nm and 60 μm of channel length and width were patterned by EBL, respectively. Afterwards the source/drain contacts (1 nm Ti/50 nm Au) were defined and deposited using e-beam evaporation technique.

The transfer characteristic of a completed GFET (Figure 8(a)) on the flexible Kapton substrate is shown in Figure 8(b). The hole and electron mobilities, extracted using a widely accepted diffusive transport model [53], are 1880 and 5170 $cm^2/V{\cdot}s$, respectively, with corresponding contact resistances of 1380 and 1830 Ω·μm for holes and electrons. Residual carrier concentrations is about $\sim 4 \times 10^{11}$ cm^{-2}, which is in good agreement with a previous study using Al_2O_3 dielectrics [26]. The asymmetric transfer characteristic is attributed to high work-function metal at source and drain, which induces additional

junction resistance in the electron branch. Electro-mechanical performances of flexible graphene FETs with NPI dielectric are shown in Figure 2.8. Device performances degrade with increasing strain due to ohmic loss at S/D contacts. Importantly, leakage current (I_G) is independent on applied strain up to 10 %. The extrinsic cut-off frequency ($f_{T,ext}$) of this device is as high as 6.5 GHz at a drain voltage of 0.5 V as shown in Figure 2.8(d). The $f_{T,ext}$ is higher than the reported value that was extracted from the similar device structure with the embedded gate and high-k gate dielectrics. The improvement in $f_{T,ext}$ can be attributed to about 3.5 times shorter channel length, significantly reduced contact resistance and parasitic capacitances between gate and drain (or source).

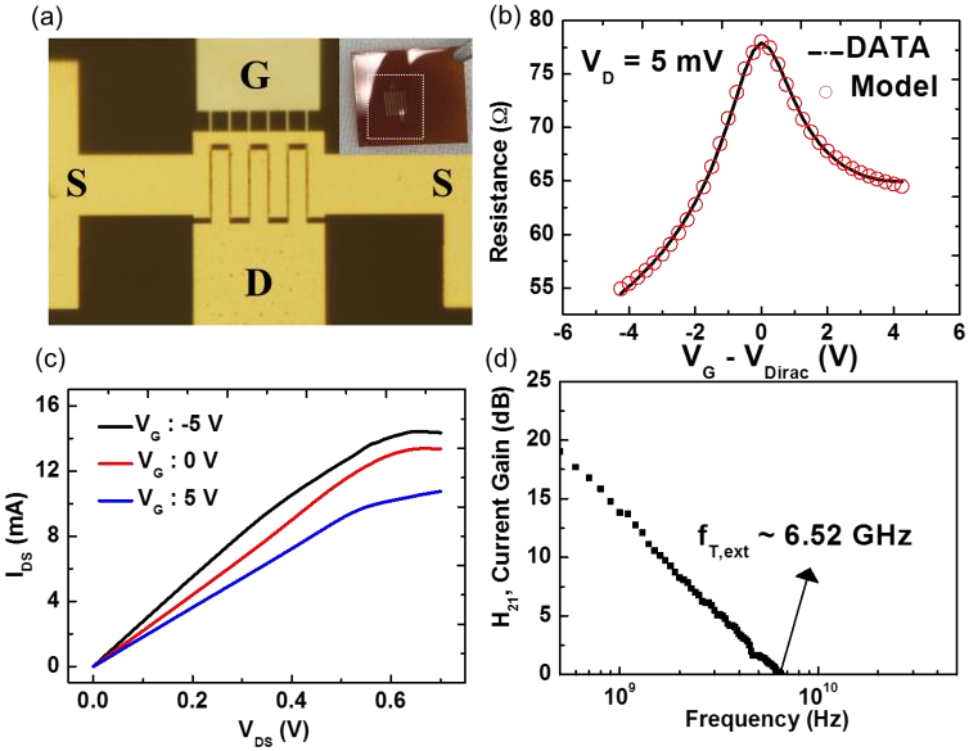

Figure 2.8: Flexible graphene transistor using nanoscale polyimide gate dielectric. (a) an optical image of the embedded-gate graphene TFTs. Channel width and length are 60 μm and 250 nm, respectively. (b) transfer characteristics of graphene TFTs with 60 nm-thick NPI gate dielectric. Extracted mobilities for hole and electron are 1880 $cm^2/V{\cdot}s$ and 5170 $cm^2/V{\cdot}s$, respectively. (c) output Characteristics with various gate voltages from -5 V to 5 V with gate voltage step of 5 V, which show weak current saturation at high fields. (d) current gain as a function of frequency. The extrinsic cut-off frequency from measured S-parameters is about 6.5 GHz.

In order to characterize electro-mechanical performances of flexible GFETs with NPI dielectric, ex-situ bending measurement was employed to characterize flexibility of NPI dielectric GFETs. (Ex-situ bending measurement indicates all electrical measurements

were characterized when the strain is not applied to the sample.) Note that bending was performed along with the channel length direction. Figure 2.9(a) represents transfer performances of GFETs with NPI dielectric after each strain. Total resistance (R_{tot}) is a sum of channel resistance and contact resistance at S/D, $R_{tot} = R_{channel} + 2 \cdot R_{contact}$ [14]. Drain bias (V_{DS}) was 5 mV. Figure 2.9(a) shows R_{tot} increases with increasing strain. However, flexible dielectric performance, in terms of mechanical breakdown and gate leakage current, was not dependent on applied strain (Figure 2.9(b)), which demonstrates the outstanding electro-mechanical stability of NPI dielectric for flexible gate dielectric. We attribute the performance degradation to increased graphene-metal contact resistance under strain, and Figure 2.9(c) shows extracted mobility in hole branch increases with increasing strain, thus, mobility degrades mainly due to the Ohmic loss at S/D.

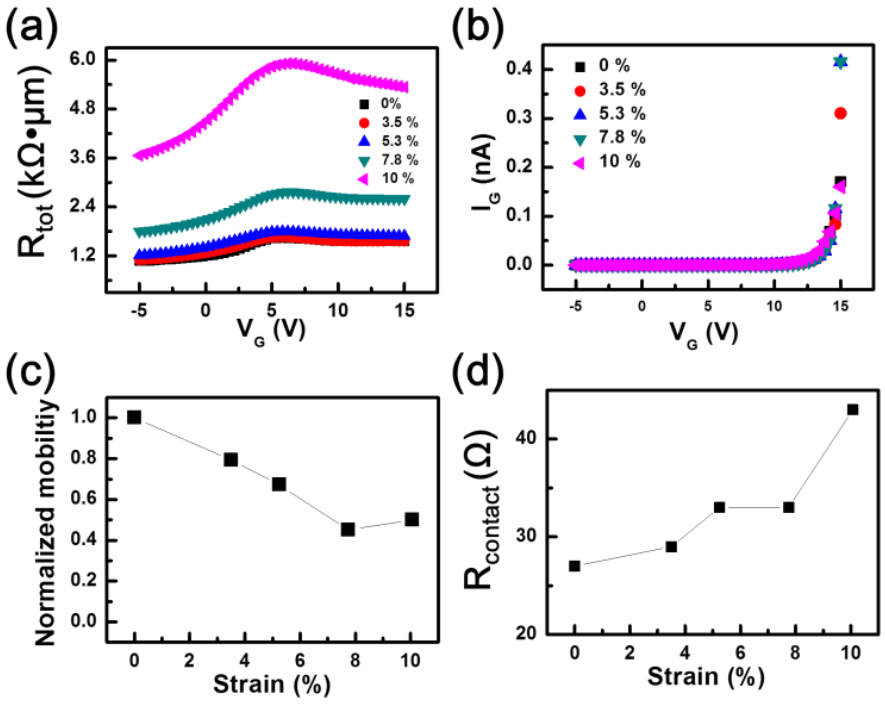

Figure 2.9: Electro-mechanical performances of flexible graphene FETs with NPI dielectric. (a) transfer characteristics of a GFET with NPI dielectric with different ex-situ strains. (b) gate leakage current during applying strain up to 10 %. (c) Mobility dependent on strain. (d) contact resistance as a function of strain.

Chapter 3: Flexible Graphene Field-Effect Transistors

GRAPHENE FIELD-EFFECT TRANSISTORS ON FLEXIBLE GLASS SUBSTRATE

Two-dimensional (2D) atomically thin graphene is highly attractive for future smart nanosystems due to its high mechanical strength, and high carrier mobility exceed 10,000 cm^2/Vs at room temperature. In particular, the fast frequency response with 100 GHz cut-off frequency demonstrated at 250 nm channel length and subsequently extended to 427 GHz at 67 nm active channel length on rigid substrates including SiO_2/Si wafers [1, 2, 54-56]. Although the short channel devices on rigid substrates are operated in the extremely high frequency spectral (EHF), range from 30 GHz to 300 GHz, comparable EHF responses on flexible substrates have not been demonstrated due to rough surface smoothness and thermal conductivity of plastic substrates such as polyethylene naphthalate (PEN), polyethylene terephthalate (PET) and polyimide (PI) [25, 26, 57, 58].

S. Park, W. Zhu, and H.-Y. Chang equally contributed all of works. S. Park contributed to write the manuscript, graphene device fabrication, RF data analysis for all devices. W. Zhu contributed to fabricate black phosphorus devices and electrical measurements. H.-Y Chang contributed to fabricate CVD MoS_2 devices and electrical measurements. M. N. Yogeesh contributed to RF data analysis discussion and electrical measurements, and R. Ghosh and S. K. Banerjee contributed to grow CVD MoS_2. D. Akinwande supervised all of the works, and all authors reviewed and commented on the results and manuscript. D. Akinwande is the corresponding author for the publication.

Contributions: S. Park carried out the device design, fabrication, and CVD graphene growth, and electrical characterization and analysis with contributions from S. H. Shin, M.N. Yogeesh, A. L. Lee, S. Rahimi, and D. Akinwande. S. H. Shin and M. N. Yogeesh contributes to discuss RF data analysis, and A. L. Lee and S. Rahimi contributes to optimize the high quality of CVD graphene. D. Akinwande supervised all of works, and all authors reviewed and commented on the results and manuscript. S. Park is the corresponding author for the publication.

PI substrate has been utilized as plastic flexible substrates thanks to its relatively high glass transition temperature (~ 400 C) and chemically inert characteristics, but thermomechanical failure is still one of the critical problems in 2D nanomaterial based flexible electronics because of the operation in saturation velocity regime for high frequency performances as described in Chapter 1 [1, 27, 58, 59]. In this chapter, we introduce (Willow) glass substrates (from Corning) as a flexible substrate by comparing with commonly-used plastic substrates. Table 3.1 represents the comparison of the characteristics of flexible substrates. Flexible glass substrate is relatively less compliant substrate, compared with PI and PET, but its higher glass transition temperature enables to facilitate the high temperature processes such as rapid thermal annealing and atomic layer deposition. Additionally, characterized RMS surface roughness is less than 0.5 nm without any post-treatments. Thermal conductivity of flexible glass substrate has about 8 times larger than commonly-used plastic substrates. Particularly, the flexible glass substrate enables high field operation without the joule heating induced substrate deformation observed on polymeric substrates.

	Young's modulus [GPa]	Glass transition temperature [ºC]	Surface RMS roughness [nm]	Thermal conductivity [W/m·K]
Flexible Glass	70 – 80	>750	<0.5	1
PI	5	<400	<1	0.12
PET	2.8 – 3.1	<200	<2	0.15

Table 3.1. Comparison of properties of flexible substrates in terms of Young's modulus, glass transition temperature, surface roughness and thermal conductivity.

Figure 3.1(a) shows a 3D illustration of graphene FETs on flexible glass. Figure 3.1(b) and 3.1(c) are an optical image of GFETs with six fingers and GSG contact pad for RF measurement and the cross-sectional view of GFETs on flexible glass substrate, respectively. The GFETs fabrication starts with EBL patterning and e-beam evaporation for an embedded gate metal stack (Ti 2nm/Au 38 nm). Solution based NPI precursor is spin-coated on embedded gate structure and cured to deposit 60 nm-thick NPI dielectric under N_2 atmosphere at 250 ºC [43, 44]. As described in Chapter 2, the measured RMS surface roughness is less than 0.5 nm. Reducing surface roughness is important to minimize disorder and enhanced charge transport in the graphene channel. CVD graphene is grown on Cu foil (APPENDIX A.1), and PMMA assisted wet transfer was employed to transfer large area graphene on Cu foil to NPI/embedded gate/flexible glass substrate [14]. Note that the NPI dielectric is not exposed to any organic residues including PMMA, which indicates we can have "clean" graphene-dielectric interface. The active graphene channel

area, device-to-device isolation, via for embedded gate pad connection and edge-injection contact were patterned followed by O_2 plasma RIE etching for graphene etch and CF_4/Ar plasma RIE for NPI dielectric (Figure 3.1(c) and Figure 3.1(d). Source and drain were completed by EBL and e-beam evaporator. The S/D contact metal consists of 1 nm-thick Ti and 45 nm-thick Au. Ti layer was used for adhesion layer between graphene and metal, and Au metal layer was employed due to its low resistivity. Note that there is the thin native TiO_2 layer on Ti metal target. Thus, the Ti metal target got heated by e-beam for an enough time before S/D e-beam deposition to prevent TiO_2 deposition on graphene-metal contact area. Device channel width and length are 60 μm and 140 nm, respectively.

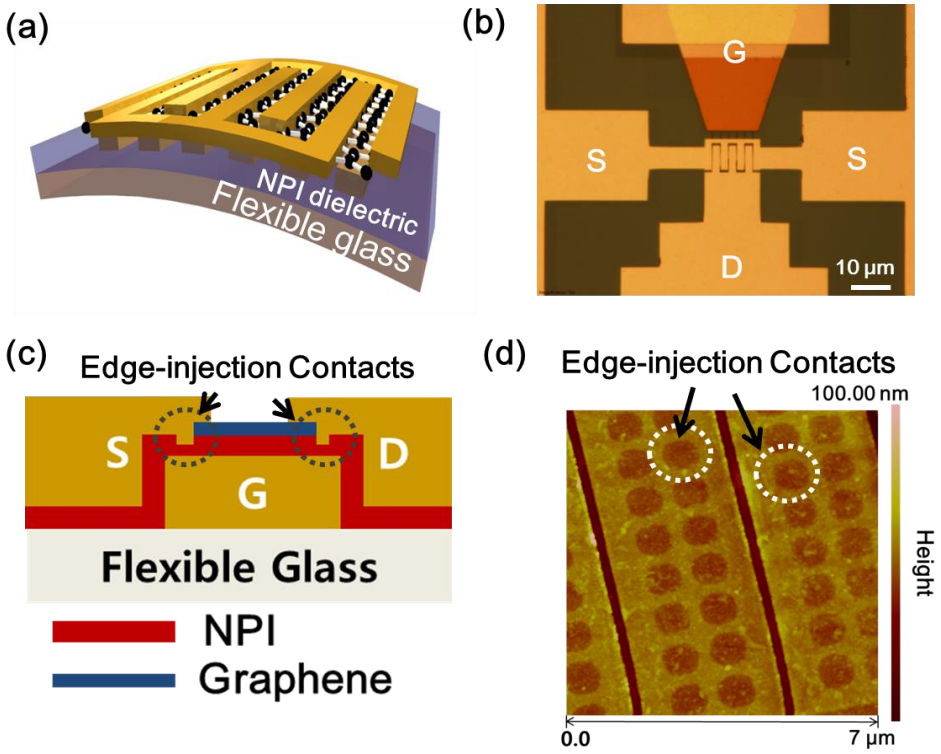

Figure 3.1: Graphene FETs on flexible glass substrate. (a) 3D illustration of embedded-gate graphene FETs. (b) an optical image of the embedded-gate graphene FETs with six fingers and GSG pads. (c) cross-sectional view of graphene FETs with edge-injection contacts. (d) an AFM image which shows topology of edge-injection contacts and 140 nm channel length.

Figure 3.2 shows DC electrical characteristics of a representative GFETs at room temperature under ambient condition. Output characteristics show linear transport at low field as well as weak current saturation at high field as shown in Figure 3.2(a). We attribute the current saturation to low surface roughness of NPI dielectric. Figure 3.2(b) is transfer characteristic of GFETs on flexible glass substrate. The drain voltage is 5 mV, and the inset shows the corresponding transconductance (mS/V). Experimental data have good agreement with the widely used diffusive transport model for GFETs. The extracted hole

(electron) mobility and contact resistance are 4540 (1100) cm^2/Vs and 1140 (720) Ω·cm, respectively. The relatively low mobility is in part due to the short channel length of the GFETs [60], and it can be improved by reducing metal-graphene contact resistance [21]. The asymmetric transfer characteristic is mostly due to the high work-function metal at S/D contact, which increases junction resistance for electron transport [21, 26].

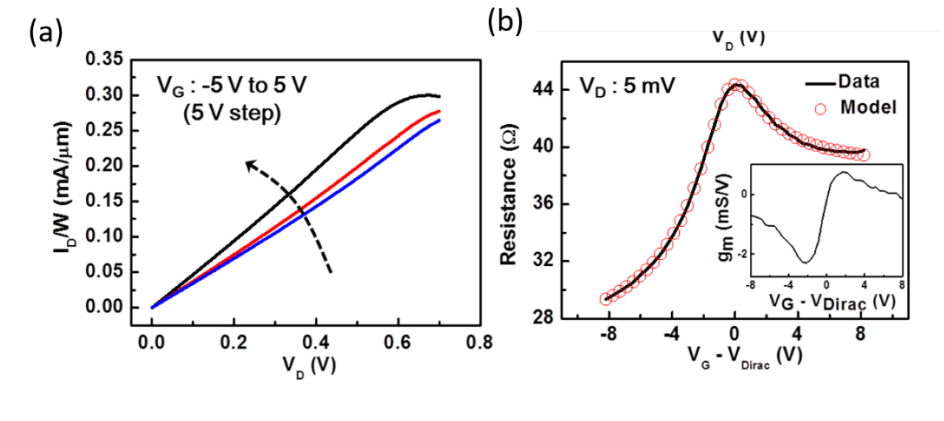

Figure 3.2: DC characteristics of GFETs on flexible glass. (a) output characteristics showing weak current saturation at high field. (b) transfer characteristics of GFETs. Inset shows transconductance (mS/V).

HIGH FREQUENCY RESPONSE

Radio frequency characteristics of the GFET with GSG pads were measured up to 30 GHz using an Agilent vector network analyzer (VNA-E8361C) after the standard short-open-load-transmission (SOLT) calibration. The standard SOLT was conducted for subtracting effects of RF cables, RF probes and stage vibration. To subtract parasitic capacitances and inductances in GSG metal pads, we characterized OPEN and SHORT measurements on the same device. Note that OPEN device has the same device structure and dimensions except for active graphene channel, which means graphene active channel

is etched by O_2 plasma after extrinsic RF performance is measured. SHORT structure requires a EBL pattern and metallization to short all three terminals. Figure 3.3(a) shows the short circuit current gain as a function of frequency, showing the 95 GHz intrinsic cut-off frequency($f_{T,int}$) at V_{DS} = 0.5 V and power gain (f_{max}) over 30 GHz, and inset shows the extrinsic current gain. Note that extrapolation line (-20 dB/dec) was fitted from 20 GHz to 30 GHz. Note that the transfer characteristic of the device is shown in Figure 3.2(b). The intrinsic/extrinsic f_T ratio is about 16, it is mostly due to significant effects of contact resistance that lower $f_{T,ext}$. Since extrapolation on a log scale can result in ambiguous $f_{T,int}$ extraction in Figure 3.3(a), the value of $f_{T,int}$ was also verified through the more accurate Gummel's method as shown in Figure 3.3(b) [61]. The imaginary part of $1/h_{21}$ is proportional to inverse slope in Figure 3.3(b), which extracts f_T about 95 GHz.

Intrinsic transconductance (g_m) is extracted from the measured extrinsic Gm (dI_d/dV_g), which has effects of source and drain metal contact resistances, via the relation for source-degenerated transistor [26]. The measured Rs and Rd are approximately 35 Ω and 11 Ω, respectively, resulting in gm of 30 μS. The intrinsic cut-off frequency can be calculated from the intrinsic g_m according to

$$f_{T,int} = \frac{g_m}{2\pi C_g W L} \qquad \text{(Equation 3.1)}$$

Since the GFET is operated in the linear region, it is expected Gm linearly increases with V_d, extracting the intrinsic g_m of 3.25 mS. Also, Cg is capacitance for active channel area, calculated to 60 nF/cm^2 for 60 nm thick NPI dielectric. Equation 3.1 yields an estimate $f_{T,int}$ ~ 95 GHz which is in good agreement with the experimental de-embedded values from S-parameters. The above three methods ascertain with confidence the outstanding RF performance of graphene TFT on glass substrate. Two related RF device metrics are worthwhile to consider for performance benchmarking, intrinsic $f_{T,}\cdot L$ and saturation

velocity (v_{sat}), which are related by $v_{sat} = 2\pi \cdot f_{T,int} \cdot L$. The extracted effective saturation velocity from f_T measurement is ~ 8.4 $\times 10^6$ cm/s. Flexible TFT device benchmarking to prior results are shown in Figure 3.3(c), highlighting the performance advantage of graphene TFT on thermally conductive flexible glass substrate affording the highest saturation velocity reported so far, from any flexible TFT on any material system [26, 57, 62-64]. The outstanding RF device metrics achieved here are attributed to (i) high thermal conductivity of substrate that can facilitate the vertical heat dissipation through substrate unlike polymeric substrates, (ii) short channel length (140 nm) so that S/D metal acts as more effective heat sinks compared to longer channel lengths, (iii) low surface roughness of gate dielectric for optimal carrier transport and (iv) low contact resistance due to edge-injection contacts and overlapped structure [65].

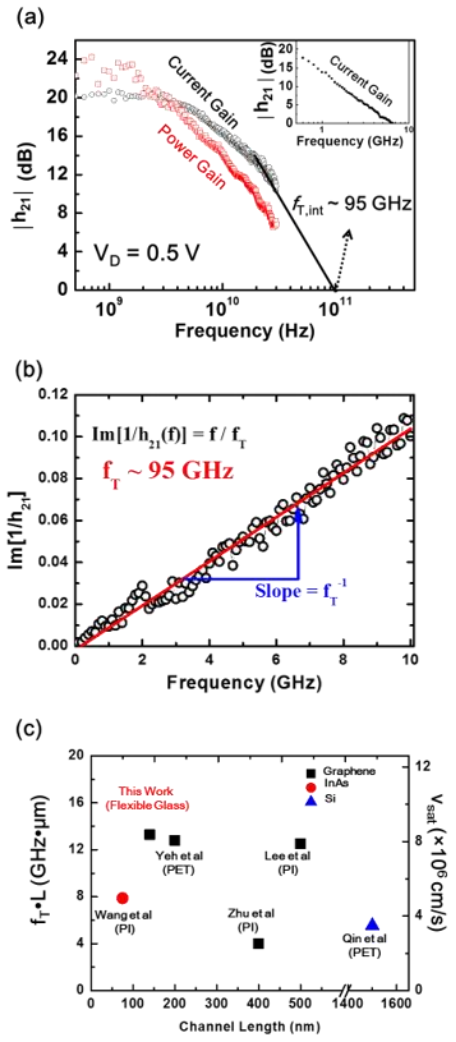

Figure 3.3: Radio frequency characteristics of GFETs on flexible glass. (a) the intrinsic cut-off frequency is ~ 95 GHz, which is 196 % higher than our previous results on polymeric substrates. The intrinsic f_{max} is at least higher than 30 GHz that is frequency limitation of our test setup. An inset shows $f_{T,ext}$, giving intrinsic/extrainsic ratio ~16, mostly due to effects of contact resistance that lower $f_{T,ext}$. (b) $f_{T,int}$ estimation by Gummel's approach. The inverse of the slope is ~ 95 ± 1.5 GHz, which is in agreement with experimental data. (c) benchmarking of flexible graphene RF device performance compared to prior results and other candidate materials [26, 57, 62-64].

To corroborate the saturation velocity obtained from RF measurement, field-dependent DC measurement of drift velocity was also used as shown in Figure 3.4. For velocity-field relationship, constants for fitting model, such as low-field mobility (μ) of 1100 cm^2/Vs, saturation velocity (v_{sat}) of ~ 8.4×10^6 cm/s as well as fitting parameter γ of 2, 3 and 4, provide good fits to the experimental data further validating the RF finding [66].

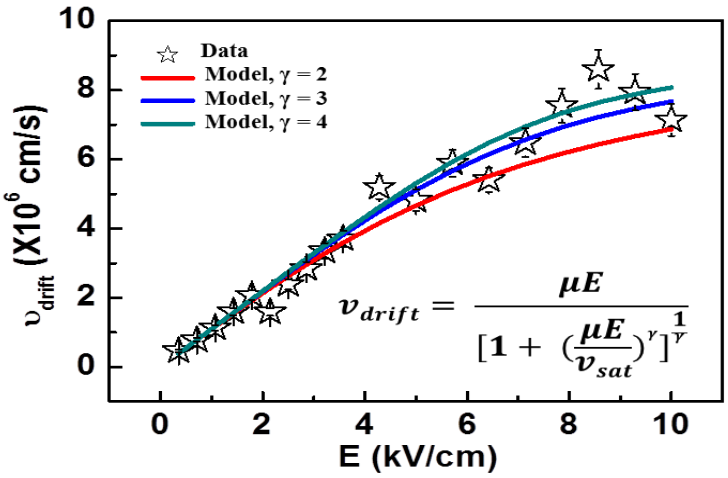

Figure 3.4: DC field-dependent measurement of drift velocity. For velocity-field relationship: constants for analytical model, such as low-field mobility (μ) of 1100 cm^2/Vs, saturation velocity (v_{sat}) of ~ 8.4×10^6 cm/s as well as empirical model parameter γ of 2, 3 and 4, provide good fits to the experimental data [66].

In this chapter, we have demonstrated graphene thin film transistors with embedded gates of six fingers with 140 nm channel length on flexible glass, which offer high thermal conductivity and surface smoothness in contrast to polymeric substrates. In addition, we developed a flexible nanoscale polyimide gate dielectric with surface smoothness comparable to rigid inorganic metal oxide dielectrics, affording reduced disorder and high frequency response. The maximum mobility and low contact resistance in electron (hole) branch are 4540 (1100) $cm^2/V{\cdot}s$ and 1140 (720) Ω·μm, and the achieved cut-off frequency

of 95 GHz is 196 % higher than the previous results on plastic substrate. The extracted saturation velocity is the highest from any flexible transistors on any material system. The outstanding RF TFT performances achieved here are primarily due to improved heat dissipation, enhanced transport and reduced contact resistance.

Chapter 4: Applications of Chemical Vapor Deposited Molybdenum Disulfide

CVD MoS_2 Field-Effect Transistors on Rigid substrates

MoS_2 is a two-dimensional (2D) semiconductor in the family of transition metal dichalcogenides (TMDs). Its single layer direct bandgap of ~1.8 eV allows for high I_{on}/I_{off} metal-oxide semiconducting field-effect transistors (FETs) [3, 17]. More relevant for radio frequency (RF) applications, theoretical studies predict MoS_2 can afford saturation velocities, v_{sat}, greater than 3×10^6 cm/s [67]. While the RF applications of MoS_2 are still in their infancy, recent studies have pushed exfoliated MoS_2 cut-off frequencies significantly higher [15, 68, 69]. The exfoliated trilayer MoS_2 that employed edge contacts achieved an intrinsic $f_{,int}$ of 25 GHz [69]. The exfoliated multilayer MoS_2 transistor used transferred gate stacks obtain an intrinsic intrinsic $f_{,int}$ of 42 GHz [15]. However, for industrial scale applications, the mechanical cleavage (exfoliation) process is not scalable and, thus far, there have been few studies on chemical vapor deposited (CVD) MoS_2 RF FETs [19, 70]. Our prior result reported demonstrated monolayer CVD MoS_2 top-gated FETs with an f_T of 6.2 GHz [70]. Furthermore, the work of transferred monolayer CVD MoS_2 on a flexible substrate to achieves the f_T of 5.6 GHz [19]. As been done with exfoliated MoS_2, novel device configurations must be applied to CVD MoS_2 to push cutoff frequencies higher.

The results described in this chapter have been published in: "Embedded gate CVD MoS_2 microwave FETs," npj 2D Materials and Applications, Vol. 1, issue 1, page 26, 2017, by A. Sanne, S. Park, R. Ghosh, M. N. Yogeesh, C. Liu, L. Mathew, R. Rao, D. Akinwande and S. K. Banerjee. Contribution: A. Sanne and S. Park equally contributes to device structure design, fabrication, and electrical measurements and analysis. R. Ghosh and L. Liu contributed to CVD MoS_2 growth and M. N. Yogeesh provided helpful discussion for RF data. L. Mathew and R. Rao helped to build all of device layout and design, and D. Akinwande and S. K. Banerjee supervised all of works. All authors reviewed and commented on the results and manuscript. A. Sanne and S. K. Banerjee are the corresponding authors for the publication

In this study, we take a step in this direction by taking an embedded gate structure to CVD MoS_2 FETs. The embedded gate transistor has been well established in literature, particularly for the most prototypical 2D material, graphene [26]. Graphene RF FETs using embedded gate transistors have achieved sub-THz cut-off frequencies [27, 28]. However, the Dirac cone band structure of graphene results in a zero bandgap, which limits current switching characteristics in graphene devices [2]. The embedded gate structure has been shown to significantly improve current saturation in graphene RF FETs, resulting in improved voltage and power gain [71]. Embedded gate FETs using CVD MoS_2 for digital circuits were recently studied, which found increased scalability, with higher yield and uniformity versus their top-gated counterparts [72]. Additionally, embedded gate CVD MoS_2 FETs show enhancement mode operation, which is essential for complex multistage integrated circuits. The common theme allowing improved performance among all 2D materials using embedded gates is a resist-free channel-dielectric interface with a reduced number of fabrication process steps after the transfer of the active material. In addition, the seed layer for ALD dielectric is not needed. Motivated by advantages described above, in this work, we employ the embedded gate structure to advance the RF characteristics of CVD MoS_2.

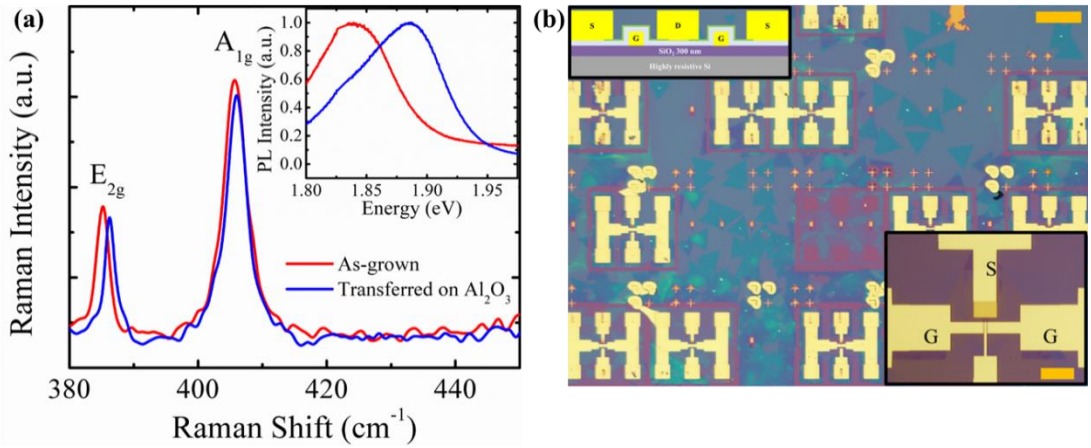

Figure 4.1: (a) raman and photoluminescence (inset) spectra before and after transfer confirming the preserved CVD MoS_2 quality. The slight shift in the in-plane vibrational mode, E_{2g}, and the blue shift in the photoluminescence peak correspond to a release of thermal mismatch induced strain after transfer. (b) optical image of a CVD MoS_2 device array with close-up gate finger layout (bottom-right inset) and a cross-sectional schematic of an embedded gate MoS_2 FET (top-left inset). The scale bar for the array (top-right) is 150 µm and the scale bar for the inset (bottom-right) is 10 µm.

Figure 4.1(a) shows the Raman spectra of the as-grown and transferred MoS_2. The slight shift in the in-plane vibrational mode, E_{2g}, corresponds to a release of strain that exists in as-grown samples due to the mismatch of thermal coefficients between MoS_2 and the SiO_2 substrate [73]. The result of the same effect is also observed in the blue shift in the peak position of the photoluminescence spectra (Figure 4.1(a) inset). Figure 4.1(b) shows an optical image of a fabricated CVD MoS_2 device array. Figure 4.1(b) inset (bottom-right) shows the zoomed-in image of the gate fingers while Figure 4.1(b) inset (top-left) is a schematic of the cross-sectional view of the embedded gate device structure.

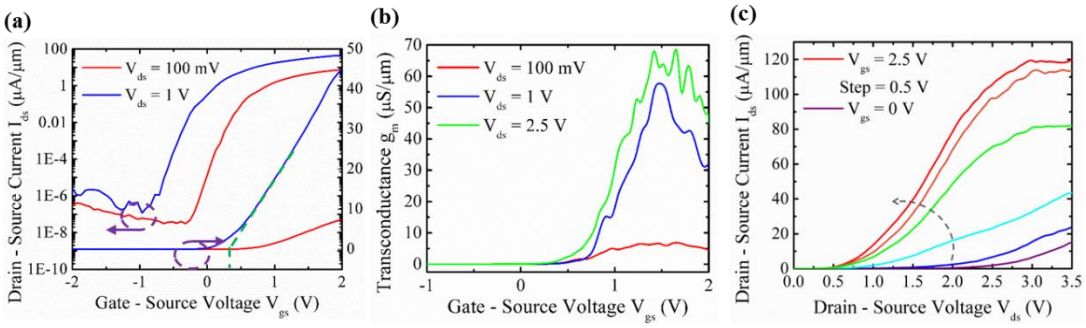

Figure 4.2: (a) transfer curves, I_{ds}-V_{gs}, for a 150 nm gate length CVD MoS_2 device. The device shows enhancement mode operation with an I_{ON}/I_{OFF} ratio of 10^8 at 100 mV of drain bias. (b) transconductance curves, g_m-V_{gs}, for the same device. The device has a peak g_m of 70 μS/μm at a V_{ds} of 2.5 V. (c) output curves, I_{ds}-V_{ds}, for the same device. The device has a current density of 120 μA/μm at a V_{ds} of 3.5 V. The device shows current saturation beyond a V_{ds} of 3 V.

Figure 4.2(a) shows the transfer characteristics (I_{ds}-V_{gs}) of an embedded gate MoS_2 FET with a physical gate length, L_g = 150 nm. The embedded gate structure preserves a clean MoS_2-dielectric interface with less fixed-charge and resist impurities [72]. As a result, the threshold voltage, V_{th}, is positive and close to 0 V, as opposed to many top-gated structures, which suffer from uncompensated charge at the surface [70]. As shown in Figure 4.2(b), we measure a transconductance, g_m, of 70 μS/μm at a V_{ds} = 2.5 V. This is the highest reported transconductance g_m on exfoliated or CVD grown MoS_2 at equivalent electric fields [19, 68-70]. The maximum field-effect mobility, μ_{FE}, is 21.2 cm^2/Vs, and after contact resistance correction is 81.6 cm^2/Vs [74]. In addition to the improved MoS_2-dielectric interface, the embedded gate structure provides improved gate control over the channel. After transfer, the MoS_2 wraps conformally to the rectangular gate fingers. The electrostatic control is improved over top-gated devices because the electric field flux

reaching the MoS_2 channel is increased at an equivalent gate voltage. As an enhancement mode device, we can sufficiently deplete the channel to achieve an I_{ON}/I_{OFF} ratio of 10^8.

Figure 4.2(c) shows the I_{ds}-V_{ds} output characteristics for the same device. The device achieves current densities of 120 µA/µm at V_{ds} = 3.5 V. There is clear current saturation beyond V_{ds} of 3 V, resulting in a drain conductance, g_{ds}, within 5 µS/µm in the current saturation region (3 V to 3.5 V of V_{ds}) which is highly desirable for the high speed operation. The sub-linear curves at low V_{ds} indicate a significant Schottky barrier. We attribute this to undoped contacts and access regions in underlapped structure. Our previous top-gated CVD MoS_2 RF FETs employed sub-stoichiometric $HfO_{1.56}$ which extrinsically doped the MoS_2 contacts and access regions. This n-doping helped reduce the contact/access resistance due to thinning of the Schottky barrier width. The difference in surface charge transfer doping between oxygen-deficient HfO_{2-x} and stoichiometric Al_2O_{3+x} has been observed and well quantified in literature [75-77]. The $Al_2O_{3.1}$ used in this study is oxygen-rich and closer to stoichiometric composition, providing minimal extrinsic doping. As a result, the extracted contact resistance for the devices in this study is R_c = 3.5 kΩ·µm, which is larger than that our sub-stoichiometric $HfO_{1.56}$ devices [70]. However, using a higher bandgap dielectric, alumina, and a carefully deposited uniform gate finger surface allows the scaling of dielectric thickness down to 10 nm. We note that in our devices the top MoS_2 is exposed to ambient, allowing further dielectric/passivation layers or sensor measurements. The substoichiometric doping effects will be discussed in the following section.

Microwave performance was characterized from 0.1-15 GHz using an Agilent two-port vector network analyzer (VNA-E8361C). To accurately subtract the effects of the parasitic capacitances and resistances in the ground-signal-ground (GSG) layout, we employed the standard de-embedding method using OPEN and SHORT measurements on the same device (Appendix A.9).

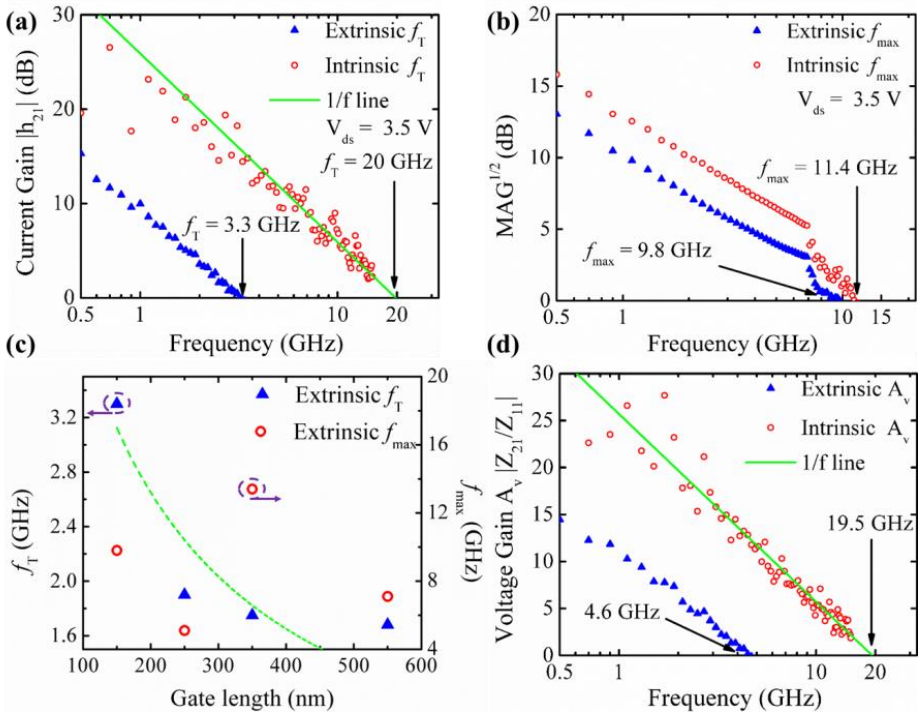

Figure 4.3: (a) short circuit current gain, $|h_{21}|$, versus frequency showing an extrinsic f_T of 3.3 GHz and an intrinsic f_T of 20 GHz. The device shows good linearity with the expected −20 dB/dec slope. (b) maximum available power gain, $MAG^{1/2}$, versus frequency showing an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. We attribute the high f_{max} to current saturation-mediated low output conductance, g_{ds}. (c) extrinsic f_T and f_{max} as a function of gate lengths from 150 - 550 nm. The dashed line is a fit of the f_T–L_g data to a 1/L line. (d) voltage gain, A_v, expressed in Z-parameters as $A_v = Z_{21}/Z_{11}$ versus frequency. The extrinsic A_v gain is unity at 4.6 GHz. After de-embedding the unity gain frequency is 19.5 GHz.

Figure 4.3(a) shows the short circuit current gain, $|h_{21}|$, as a function of frequency. Operating at V_{DS} = 3.5 V with L_g = 150 nm, we achieve an extrinsic f_T of 3.3 GHz and, after de-embedding, an intrinsic f_T of 20 GHz. The intrinsic f_T is corroborated with the Gummel approach, as shown in Figure 4.4 [61].

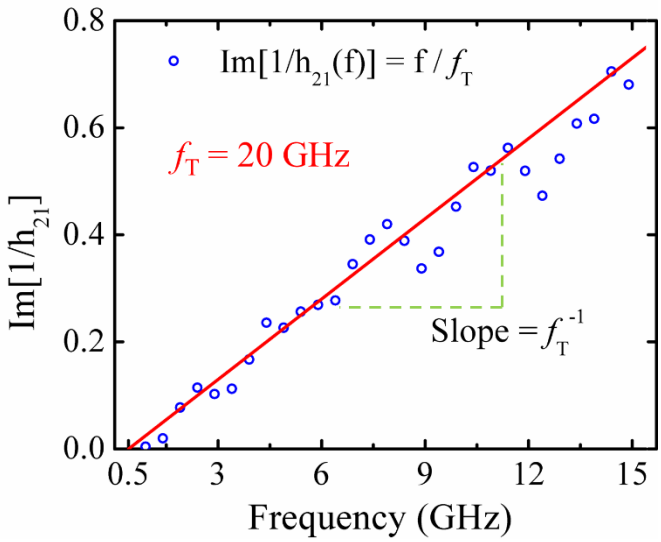

Figure 4.4: The Gummel plot confirms the 20 GHz f_T given by the inverse of the slope.

The lateral electric field used for f_T measurement is in the high-field limit where carrier transport is determined by $v_{sat} = 2\pi \cdot f_{T,int} \cdot L_g$, and in our device is 1.88×10^6 cm/s. This is the highest extracted v_{sat} for any MoS_2 RF FET at room temperature, either exfoliated or CVD MoS_2 (Table 4.1). The higher f_T can be achieved by improving the g_m (by shortening the L_g), optimizing the layout or the device structure to reduce parasitic capacitances, and reducing the contact resistance.

MoS_2 FETs Radio Frequency Comparison							
Device	Configuration (Growth method/Substrate/Structure)	f_T ext/int (GHz)	f_{max} ext/ int (GHz)	A_v ext/ int (GHz)	L_g (nm)	V_{DS} (V)	v_{sat} ($\times 10^6$ cm/s)
This Work	CVD Monolayer/Si/ Embedded gate	3.3/20	9.8/11.4	4.6/19.5	150	3.5	1.88
[69]	Exfoliated Trilayer/Si/ Top gate	6/25	-/16	-/45	70	2.5	1.1
[15]	Exfoliated 2-7nm-thick/Si/ Transferred gate	-/42	-/50	-/-	68	5	1.79
[19]	CVD Monolayer /Flex/ Top gate	2.7/5.6	2.1/3.3	-/-	500	2	1.76
[70]	CVD Monolayer /Si/ Top gate	2.8/6.7	3.6/5.3	3/11	300	3.5	1.26

Table 4.1: Comparison of RF MoS_2 FETs performance in literature. The saturation velocity (v_{sat}), calculated from intrinsic f_T, is the highest reported to date for both exfoliated and CVD MoS_2 RF systems.

Another important figure of merit for high performance transistors is the maximum frequency of oscillation, f_{max}. This is the frequency limit at which there is power gain, given matched input and output impedances. Figure 4.3(b) shows the maximum available power gain versus frequency. Operating at the same DC bias, we measure an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. This is the highest extrinsic f_{max} for all MoS_2 and the highest intrinsic value for CVD MoS_2. We attribute the high f_{max} to good current saturation, leading to a small g_{ds} and a large output resistance, r_o. Mason's unilateral gain, U_g, is shown in Figure 4.5, which is 10.3 GHz.

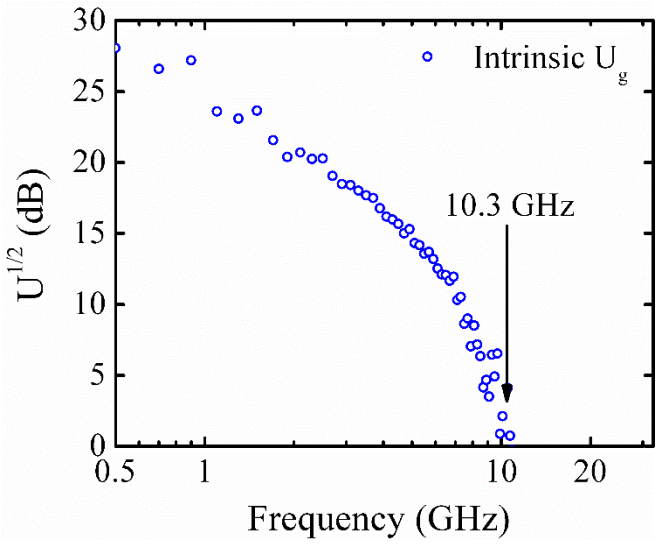

Figure 4.5: Mason's unilateral gain vs. frequency. We measure a cutoff frequency of 10.3 GHz.

Figure 4.3(c) shows the scaling of f_T and f_{max} with gate length. In the high-field limit, the f_T generally scales inversely with length while f_{max} does not follow any trend due to varying

individual device gate resistance and output conductance. In RF circuit design, it is important to know the intrinsic voltage gain A_v. The general expression for A_v is g_m/g_{ds}, but it can also be measured with impedance Z-parameters. Figure 4.3(d) shows the extrinsic and intrinsic unity voltage gain cutoff frequency as 4.6 and 19.5 GHz, respectively. The outstanding RF device performance achieved here can be attributed to (i) a resist-free MoS_2-dielectric interface, (ii) a reduced number of fabrication process steps after transfer, compared with a top gate flow, and (iii) current saturation leading to a large r_o.

Performance variability is an important factor in obtaining high yield with device-to-device uniformity on a large-scale RF transistor integration. The origin of the variation in the fabrication process presented here include intrinsic material non-uniformity, e-beam lithography, and local differences in the various device capacitances. In order to improve uniformity and coverage, gas based growth system, such as metalorganic chemical vapor deposition (MOCVD), is required [78]. Table 4.2 shows some insight into the variability and scalability of our CVD MoS_2 RF devices. We note that poor CVD MoS_2 results in non-functioning devices.

Device Count	Maximum Current (μA/μm)	g_m (μS/μm)	μ_{eff} (cm^2/Vs)	I_{ON}/I_{OFF}	Extrinsic f_T (GHz)
1	44.8	58.8	25.9	3×10^8	3.25
2	22.4	43.1	21.36	3×10^8	2.38
3	1.63	3.45	1.6	1×10^3	0.19
4	0.67	1.32	0.49	7×10^3	0.07
5	15.5	28.6	12.8	8×10^6	1.58
6	3.62	8.68	3.2	4×10^7	0.48
7	9.52	16.15	6.5	5×10^8	0.89
8	0.07	0.13	0.05	1×10^2	0.01
9	35.6	44.2	21.4	1×10^8	2.44

Table 4.2: Performance variation of device-to-device of fabricated CVD MoS_2 RF FETs.

CVD MoS_2 Field-Effect Transistors on Flexible Substrates

In this section, CVD MoS_2 FETs on flexible polyimide substrate will be introduced. As advantages of embedded gate structure for CVD MoS_2 FET are described in the previous section, we also employed the gate first approach for resist-free interface between CVD MoS_2 and gate dielectric as well as gate dielectric scalability. By applying and curing liquid polyimide on 5 mil-thick Kapton substrate, we could reduce surface roughness (RMS roughness less than 1 nm) to realize atomically thin CVD MoS_2 transistors. The embedded gates were patterned by EBL, followed by an e-beam deposition of Cr(1.5 nm)/Au(18.5 nm) stack. Then we employed ALD to deposit 10 nm-thick Al_2O_3 at 200 ºC, and CVD MoS_2 grown on the SiO_2/Si wafer is transferred on Al_2O_3/Gate/PI substrate via PMMA assisted wet transfer. More detailed wet transfer method is described in Appendix A.4. Figure 4.6(a) shows the transferred CVD MoS_2 on Al_2O_3/Gate/PI substrate. Scale bar is for 200 μm. Figure 4.7 represents single crystalline MoS_2 transferred on a gate array. Many of short gate were patterned in order to select conformally transferred MoS_2 among non-continuous CVD MoS_2 (Figure 4.6(a)). The second EBL was used to pattern VIA followed by Cl_2/O_2 plasma etching to remove unnecessary MoS_2 that impedes the wet etching process for Al_2O_3 VIA. Then the sample is dipped into the TMA developer to etch Al_2O_3 for 10 mins followed by IPA rinse. Active MoS_2 channel was defined by third EBL followed by Cl_2/O_2 plasma etching. The final EBL process was used to define short channel S/D, and Ni(15nm)/Au(25nm) was deposited for S/D contact. Figure 4.6(b) shows 3D

illustration of embedded gate CVD MoS_2 FETs with overlapped configuration, and Figure 4.6(c) represents the cross-sectional view of MoS_2 transistors on polyimide substrate.

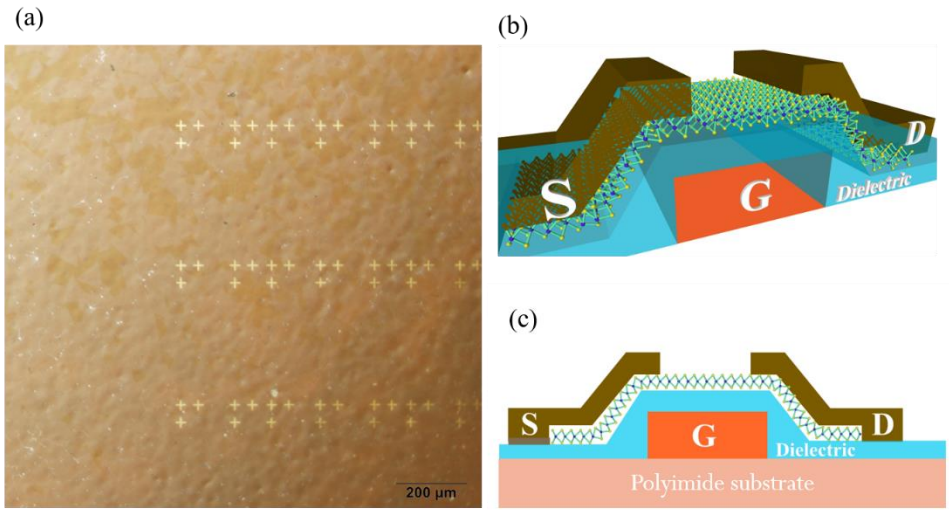

Figure 4.6: Large area CVD MoS_2 FETs with embedded gate structures. (a) an optical image for transferred CVD MoS_2 on Al_2O_3/Gate/PI substrate. (b) 3D illustration of CVD MoS_2 FETs with embedded gate structure. S/D and gate are overlapped to reduce contact resistances. (c) cross-sectional view of flexible CVD MoS_2 FETs.

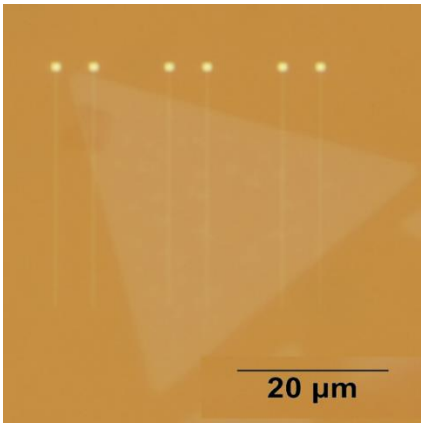

Figure 4.7: Transferred CVD MoS_2 on a gate array. The gate array is composed of 3 embedded gate sets to choose conformally transferred MoS_2.

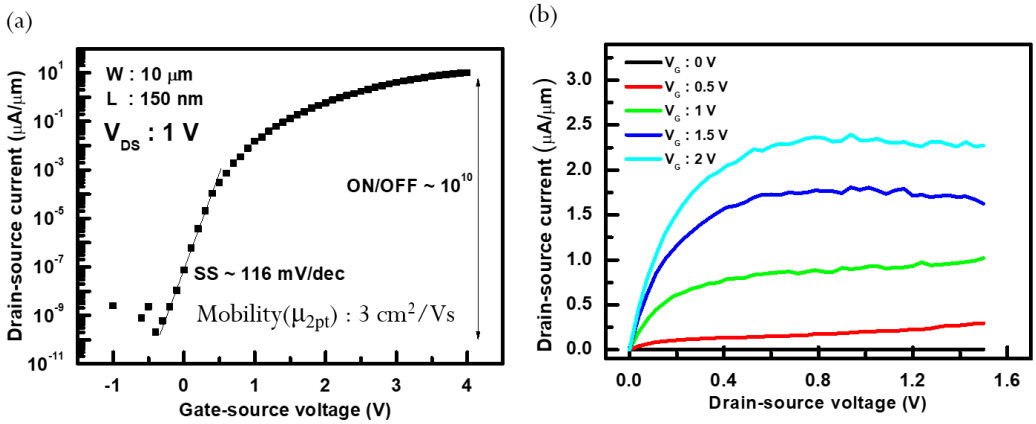

Figure 4.8: DC characteristics of CVD MoS_2 FETs. (a) transfer characteristic of CVD MoS_2 FETs on PI substrates at V_{DS}=1V. Current ON/OFF radio is over 10^{10}, subthreshold swing is ~116 mV/dec, and extracted 2-pt mobility is ~ 3 cm^2/Vs. (b) output characteristics of the short channel CVD MoS_2 transistor, showing linear transport at low field regime due to ohmic contact and current saturation at high S/D electric field.

Figure 4.8 shows DC characteristics of flexible CVD MoS_2 FETs on polyimide substrate. Chanel length (width) is 150 nm (10 μm), respectively. Transfer characteristic is

shown in Figure 4.8(a), and the current on/off ratio is over 10^{10} at V_{DS}=1V, subthreshold swing is ~ 116 mV/dec, and extracted 2-point mobility is ~ 3cm^2/Vs. Figure 4.8(b) represents output characteristics that show ohmic behavior at low S/D electric field, and stable current saturation at high field. Thanks to the overlapped structure as well as Ni contact to MoS_2, the ohmic contact behavior could be achieved.

We also employed the sub-stoichiometric HfO_{2-x} doping layer to improve current density of CVD MoS_2 FETs. Note that the active MoS_2 channel is exposed to the air in embedded gate structure.

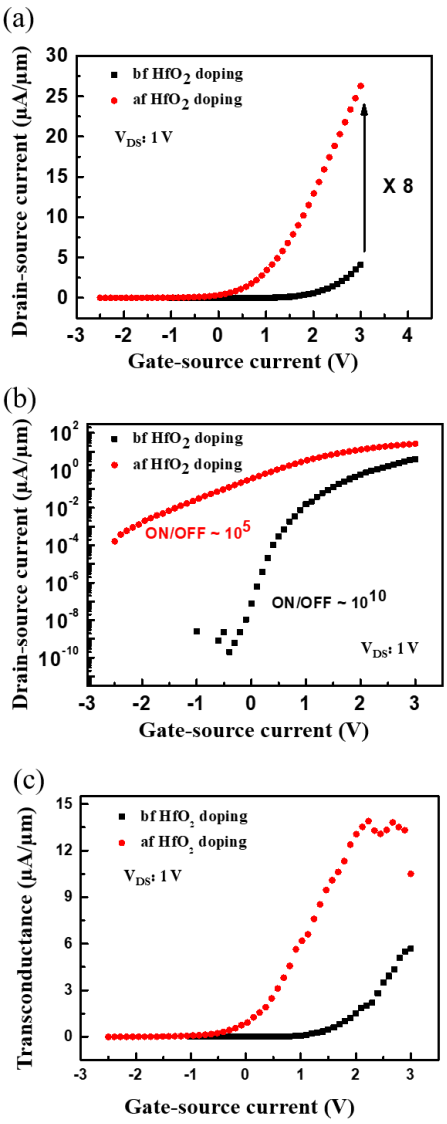

Figure 4.9: Effects of the substoichiometric doping layer on DC performances. (a) transfer characteristic in linear scale. Drain-source current density shows ×8 higher current density as well as enhancement mode operation after HfOx substoichiometric doping. (b) transfer characteristic in log scale. Degradation of current switching characteristic due to the doping effect. (c) transconductance is ×2 improved thanks to HfO_2 stoichiometric doping layer.

Figure 4.9 shows effects of O-deficient substoichiometric doping layer on MoS_2 channel. Figure 4.9(a) shows transfer characteristic before and after HfO_2 deposition in linear scale. After doping layer, the current density improves more than 8 times, and the device still operates in the enhancement mode. However, Figure 4.9(b) shows the degraded current on/off ratio (from 10^{10} to 10^5) at V_{DS}=1V. This is mostly due to Oxygen deficient doping of MoS_2, and more strong surface potential is needed to deplete charge carriers in channel. Figure 4.9(c) shows x2 improved transconductance, which is beneficial for RF performances.

Chapter 5: Two-Dimensional Material Based Paper Electronics

Commercially available paper has been used as an electronic substrate, thanks to its flexible, eco-friendly, and cost-effective features as shown in Figure 5.1 [79-82]. Particularly, due to its low-cost manufacturing price, there have been many realizations for large production of organic thin film transistors on paper substrate [79]. However, compared with other flexible substrates including flexible glass, plastic substrates and stainless steel, paper substrates suffer from wet process and low thermal margin. Furthermore, there have been sparse studies on flexible 2D nanoelectronics on paper substrates. In this chapter, we utilize PI coating layer to enable wet process and conventional thermal process including ALD. In addition, we demonstrate CVD large-area monolayer graphene and MoS_2 FETs on paper substrate with high-mobility, record cut-off frequency, and flexibility for the first time [83]. These results inspire greater device research and development on ubiquitous paper platforms that can be roll-to-roll (R2R) manufactured.

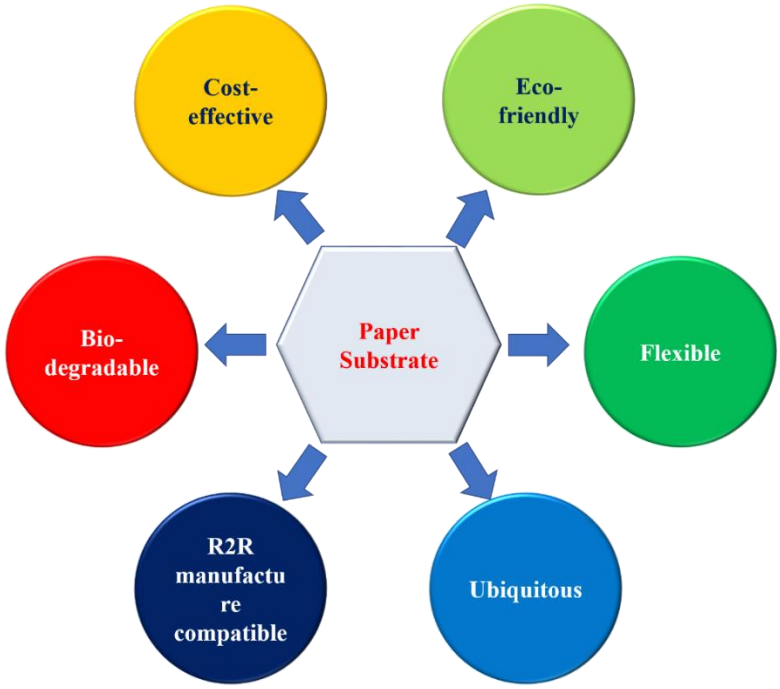

Figure 5.1: Six indispensable features of paper substrate. Paper substrates are cost-effective, eco-friendly, flexible, ubiquitous, biodegradable, and R2R manufacturing compatible.

PREPARATION OF PAPER SUBSTRATES

Commercially available glossy paper (made from wood) is characterized via atomic force microscope (AFM) for surface roughness as shown in Figure 5.2(a). It shows quite rough surface that can induce big variations in device dimensions (channel length, width, capacitance) as well as performance. In order to prevent the uncertainties and variability, reducing the surface roughness with smoothing layers for compatible roughness regime is one of the key issues for high yields and stable operation [79-81]. In this study, we employ liquid polyimide (PI-2574 from HD Microsystems, ~ 15 μm) and cured at 230 ºC under vacuum condition to improve the surface smoothness for reliable device performances

comparable to electronic-grade conventional substrates [27, 58]. AFM topologies before and after PI smoothing layer coating are shown in Figure 5.2(a) and Figure 5.2(b). For 10 μm by 10 μm (1 μm by 1 μm) scan size, the characterized root mean square (RMS) roughness is improved from 11.9 nm (4.3 nm) to 3.1 nm (1.81 nm) (Figure 5.2(c)), and the highest peak-to-peak distance reduces from 100 nm to 14 nm (Figure 5.2(d)). Table 5.1 shows a comparison of the surface roughness of paper substrates and smoothing material between previous reports and this study. Compared with other coating materials, PI provides the smoothest surface on paper substrates for device fabrications.

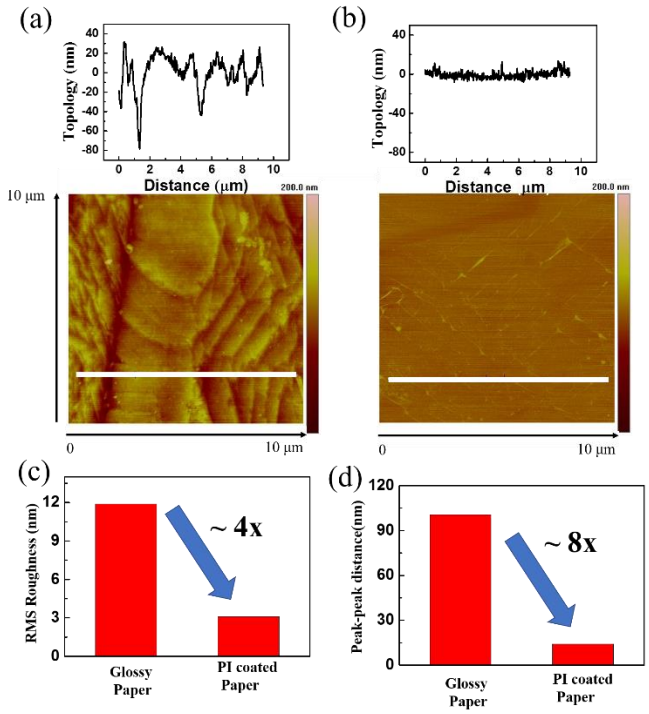

Figure 5.2: AFM characterization for surface topology before and after polyimide film on paper substrates. Surface scan (10 m by 10 m) of (a) as purchased glossy paper used in this study, and (b) after PI film smoothing layer. Topological scan along with the white line in (a) and (b) shows huge improvement of the surface roughness after Pi coating layer with respect to (c) surface RMS roughness and (d) maximum peak-to-peak roughness.

	RMS roughness [nm]	Coating layer
[79]	150	Silver Paste
[80]	7.03	Parylene
[81]	*2.01	Chitosan
Commercial Glossy paper	11.4	N/A
PI/ Commercial Glossy paper [this work]	3.11/*1.81	Polyimide

Table 5.1: Comparison of surface roughness and smoothing layer between reported literature and this study. Polyimide layer helps to reduce roughness from 11.9 nm to 3.11 nm.

In order to study surface roughness effects of paper substrates on 2D material performances, we transfer CVD graphene grown on Cu foil on bare glossy paper and PI coated paper substrates via commonly used PMMA-assisted wet transfer (more details in Appendix A2) and bake it at 90 ºC for 2 hrs at ambient condition [14]. After acetone rinse to remove PMMA layer, we employed shadow mask and e-beam evaporator to deposit metal contacts (1.5 nm Ti/38.5 nm Au) to complete two terminal graphene devices. The electrical characteristic (resistance as a function of channel length) for graphene device on paper substrates is shown in Figure 5.3(a). Graphene device on smooth PI coated paper

shows lower sheet resistance and reduced variation. Figure 5.3(b) represents the electro-mechanical bending characteristic comparison. For the graphene samples on rough paper substrates, we observe more prominent degradation of resistance at severe bending conditions less than 1.4 cm bending radius.

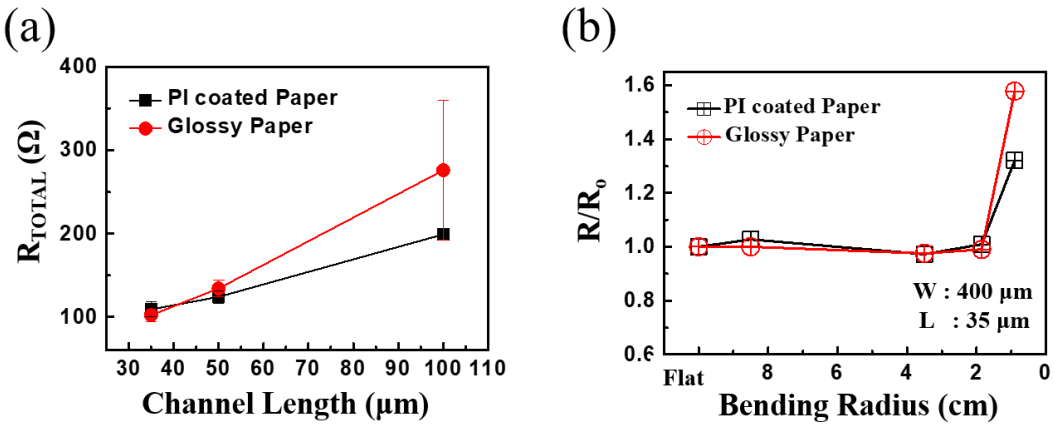

Figure 5.3: Performance comparison of two-terminal graphene device on bare glossy paper and PI coated glossy paper. Device has 400 μm width (a) total resistances, including channel resistance and contact resistance, as a function of channel length. Graphene devices on polyimide coated paper substrates shows reduced variation and lower sheet resistance. (b) electro-mechanical bending test. More prominent degradation of resistance on rough device is observed.

GRAPHENE FIELD-EFFECT TRANSISTORS ON PAPER SUBSTRATES

An array of graphene field effect transistors (GFETs) employing CVD monolayer graphene were fabricated on PI coated paper substrate as shown in Figure 5.4(a). Embedded gates were patterned EBL followed by metal deposition (2 nm Cr/18 nm Au). ALD Al_2O_3 (15 nm) was used for gate dielectric. Graphene is transferred via PMMA-assisted wet transfer, and it is patterned and etched to isolate active graphene channel. S/D EBL patterns

and metallization (Ni 15 nm/Au 25 nm) are done to complete device fabrication. Channel length (width) is 250 nm (10 µm). A representative transfer characteristic is shown in Figure 5.4(b). Dirac voltage is near 0 V, and the diffusive transport model is utilized to extract mobility and contact resistance in hole and electron branch [53]. The extracted hole (electron) mobility is ~3600 (2380) cm^2/Vs, and contact resistance in hole (electron) branch is 915 (1060) Ω·µm, which are comparable or slightly better than other studies on rigid and flexible GFETs [14]. Output characteristics are shown in Figure 5.4(c) with record current density on paper based on 2D atomic materials (Table 5.2).

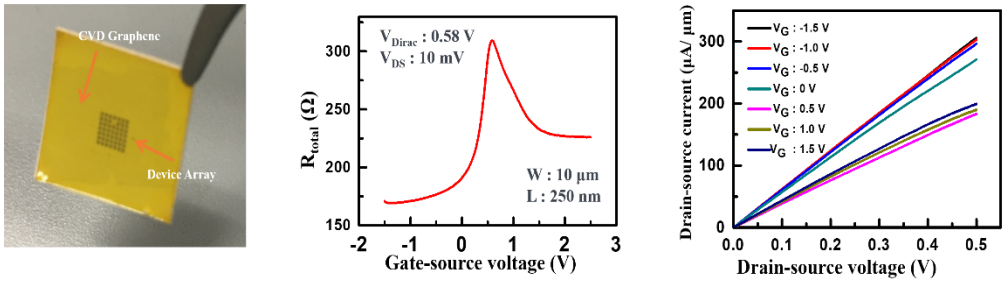

Figure 5.4: Graphene field effect transistors on PI coated paper substrate. (a) an image of CVD graphene device array on PI coated paper substrate. (b) transfer characteristic of graphene FETs. Channel length (width) is 250 nm (10 µm). The diffusive transport model is employed to extract device parameters, and the extracted hole (electron) mobility is ~ 3600 (2380) cm^2/Vs and contact resistance in hole (electron) branch is 915 (1060) Ω·µm. (c) output characteristic of graphene FETs on paper substrate. Current density at V_{DS} of 0.5 V is ~300 µA/µm with record current density on paper based on 2D atomic materials

	This work	[79]	[81]
Channel Material	Graphene	DNNT	P3HT
L [μm]/ W[μm]	0.2/20	60/6000	80/1600
Channel Thickness [nm]	<0.5	5	N/R
Max current density [μA/μm]	300	0.016	~ 1
Bending radius [cm]	0.6	N/R	1.7

Table 5.2: Comparison of device structure, performance and flexibility. N/R is not reported

Figure. 5.5 shows electro-mechanical bending measurements of graphene FETs on paper substrates. Stable transfer characteristics under 1,000 bending cycles at 0.6 % strain indicates comparable performances and flexibility of GFETs on paper substrates (Figure 5.5(a)). Figure 5.5(b) shows transfer characteristics of graphene FETs while under bending strain. The GFETs show stable electrical characteristics measured till bending radius ~1.4 cm. We attribute the slight variation of transfer characteristics under bending to contact pad probing issues on compliant PI coated paper substrates.

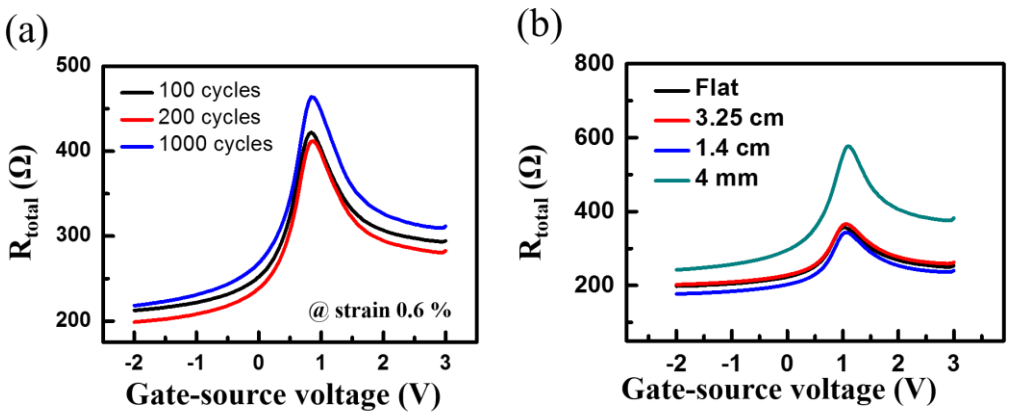

Figure 5.5: First demonstration of electro-mechanical bending measurement of graphene FETs on paper substrate. (a) transfer characteristics under bending cycling tests. It shows robust electrical performance measured till 1,000 cycles at 0.6 % strain. (b) transfer characteristics of graphene FETs while under bending strain. The graphene FET shows stable electrical characteristics measured till bending radius ~1.4 cm, which indicates R2R manufacturing compatible paper substrate for massive production.

The first RF performances of graphene FETs on paper substrate were characterized using VNA as shown in Figure 5.6(a) and 5.6(b). Figure 5.6(a) shows current gain as a function of frequency at V_{DS}=0.7 V. The intrinsic cut-off frequency ($f_{T,int}$) is ~25 GHz, which is corroborated with Gummel's plot (Figure 5.6(b)) [60]. The inverse slope of the Gummel' plot is $f_{T,int}$, 24.7 GHz ,which is well matched to the extrapolated f_T from measured S-parameters. The RF finding shows that flexible graphene FETs on paper substrates can be used for low-cost ubiquitous and/or disposable smart wireless nanosystems or IoT applications.

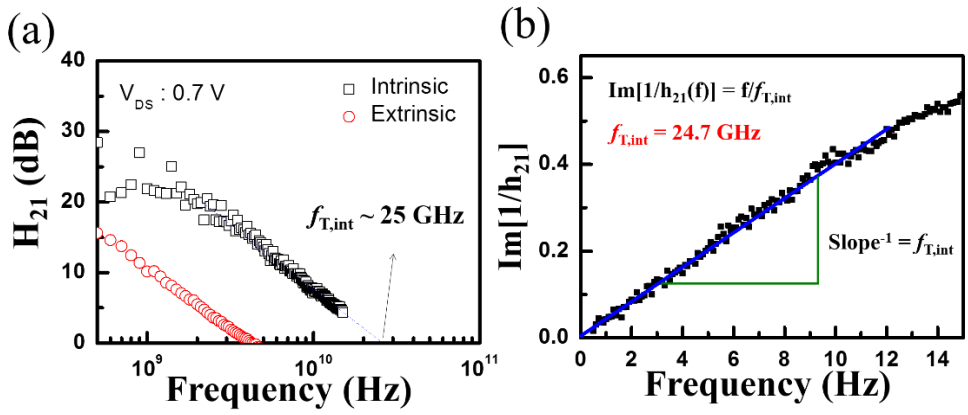

Figure 5.6: Radio frequency characteristics of graphene FETs on paper substrate. (a) current gain as a function of frequency, converted from measured S-parameters. The intrinsic cut-off frequency ($f_{T,int}$) is ~ 25 GHz after standard de-embedding process (open and short) to remove pad parasitic effects. (b) Gummel's plot confirms the de-embedded RF performances. The inverse of the slope in (b) is ~24.7 GHz that is well matched to extrapolated $f_{T,int}$ finding in (a), and represents record 2D FET RF performance.

MOLYBDENUM DISULFIDE TRANSISTORS ON PAPER SUBSTRATES

Large area CVD MoS_2 on SiO_2/Si substrates was characterized via Raman and photoluminescence (PL) measurement. The gap between E_{2g} and A_{1g} peaks is ~ 21cm^{-1}, and we obtained PL peak at 1.85 eV, which indicates high quality monolayer CVD MoS_2. [1, 70, 76] The characterized CVD MoS_2 was transferred on Al_2O_3 gate dielectric of embedded gate structure. Active MoS_2 channel was defined by EBL and CF_4 and Ar plasma etching, followed by EBL and e-beam evaporation for S/D metal contacts consist of 10 nm Ni/30 nm Au. Semiconductor parameter analyzer (B1500) was employed to measure transfer and output characteristics (Figure 5.7(a), (b)) of CVD MoS_2 FETs on paper substrates. Figure 5.7(a) shows comparable DC performances including I_{ON}/I_{OFF} > 10^9, maximum

transconductance ($G_{m,MAX}$), ~5 μS/μm at V_{DS} = 1 V, and two point field effect mobility ~6 cm^2/Vs at V_{DS}= 0.1 V. Figure 5.7(b) represents the output characteristics, and it shows the Schottky barrier at low field regime, which is mainly due to underlapped gate structure, not due to Ni/Au contact (the inset shows Ohmic characteristics of Ni/Au contacts of CVD MoS_2 FETs on SiO_2 substrate with overlapped gate structure).

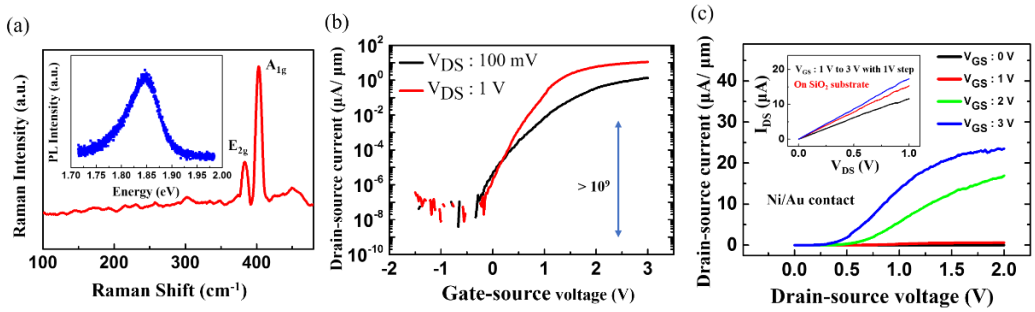

Figure 5.7: CVD MoS_2 FETs on paper substrate. (a) raman and photoluminescence measurement on CVD MoS_2/SiO2 substrate. The gap between E_{2g} peak and A_{1g} is ~ 21 (cm^{-1}), and PL peak is observed at 1.85 eV, which indicates monolayer CVD MoS_2. (b) transfer characteristics. I_{ON}/I_{OFF} ratio is over 10^9, and maximum transconductance ($G_{m,max}$) is employed to extract two-point extrinsic mobility (μ_{2pt}), 6 cm^2/Vs (including the effects of contact resistance, intrinsic mobility will be higher). (c) output characteristics of CVD MoS_2 FETs on paper. It shows Schottky barrier at low field regime, which is mainly due to underlapped gate structure and surface roughness. The inset shows Ohmic characteristics of CVD MoS_2 FETs on SiO_2 substrate (< 0.5 nm surface roughness) with overlapped gate structure.

Electro-mechanical bending characteristics of CVD MoS_2 on paper substrates is shown in Figure 5.8, displaying robust electrical performance before and after 10,000 bending cycles at 0.6 %.

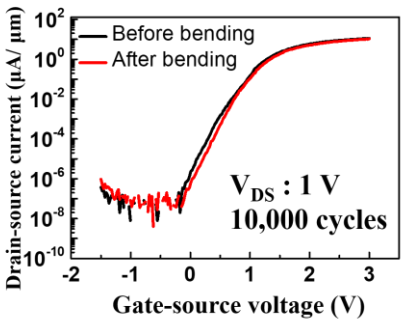

Figure 5.8: Electro-mechanical bending measurement of CVD MoS_2 on paper substrate. It shows robust electrical performances before and after 10,000 bending cycles at 0.6 % strain.

Microwave power gain (f_{max}) of CVD MoS_2 on paper substrates was characterized using GSG pad and VNA, resulting in the extrinsic f_{max} of 7.2 GHz as shown in Figure 5.9. The sudden power gain drop around 7 GHz is due to the stability factor >1 around the frequency.

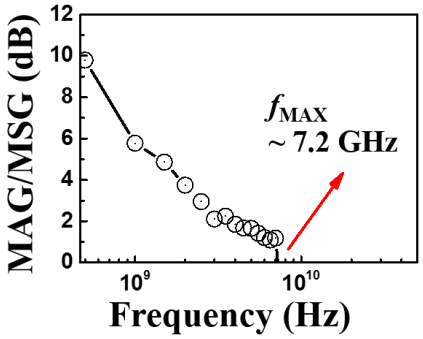

Figure 5.9: RF power gain (f_{max}) of CVD MoS_2 on paper substrate. The extrinsic f_{max} is 7.2 GHz,which is the first GHz power gain operation on paper substrates, and the sudden power gain drop around 7 GHz is due to the stability factor (>1).

Chapter 6: Summary

In this work, we have realized the high frequency 2D materials-based field-effect transistors on flexible substrates. In order to improve flexibility of transistors, we have proposed the transparent nanoscale polyimide dielectric that shows stable electrical characteristics under 10 % of strain and more than 84 % of transparency over visible light wavelength range. The transparent and ultra-flexible nanoscale dielectric is applied to graphene and MoS_2 transistors, resulting comparable device performances with high-k dielectric based 2D transistors. We have also demonstrated the short channel CVD graphene transistors on flexible willow glass that has 8 times higher thermal conductivity that prevent permanent deformation issues of plastic substrates and enable to apply high S/D field for the operation of saturation velocity regime. We employed the nanoscale polyimide dielectric as a gate dielectric, and we patterned the charge injection edge to reduce contact resistance. As a result, we represent the highest saturation velocity (8.4×10^6 cm/s) in any flexible transistors so far. For digital/logic application, we have employed large area CVD MoS_2 with the embedded gate structure on the SiO_2/Si substrate. The device shows the enhancement operation, current on/off ratio over 10^8 and the highest saturation velocity (1.8×10^6 cm/s) in any MoS_2 transistors. For the flexible digital/logic applications, we also show the embedded gate CVD MoS_2 on flexible polyimide substrate, which shows the current on/off ratio over 10^{10} and 2-point transconductance (6 μS/μm). The devices were employed to study effects of sub-stoichiometric doping of HfO_2-x. After the doping layer on embedded gate CVD MoS_2 transistors, the current density improves more than 8 times, and about 4 times better transconductance, which will be beneficial to improve RF performances. Finally, we have demonstrated GHz operation of 2D transistors on commercially available paper substrates. In order to use paper substrates for short

channel length device fabrication and to reduce surface roughness of bare paper, we applied the 15 μ-thick polyimide layer on the commercial glossy paper. CVD graphene transistors are demonstrated on PI coated paper substrate, which shows the highest current density in paper electronics, high mechanical stability, and 25 GHz of intrinsic cut-off frequency. The first CVD MoS_2 transistors on paper substrate shows the current on/off ratio over 10^9, high mechanical stability and GHz power gain. These 2D materials-based transistors shows GHz operation which can be implemented for flexible nanoelectronics systems, sensors and Internet of Things.

Appendices

A.1. Chemical Vapor Deposition Graphene Growth

Step	Details
1	Piranha cleaning thermally oxidized SiO_2/Si wafers
2	Deposit 1 µm-thick Cu film on cleaned wafers using CHA#1
3	Cleave Cu/SiO_2/Si wafers for the desired sample size. Usual sample size is 1 cm × 1cm for transistor applications or 0.5 cm × 4 cm for graphene dry transfer.
4	Load samples in the Black Magic. For the loading location, See Figure A.1.
5	Wait until base pressure below 5 mTorr
6	Run Recipe
7	Wait until chamber temperature at room temperature (usually overnight)
8	Take out samples followed by raman characterization
9	Run dummy recipe to clean the chamber for next users

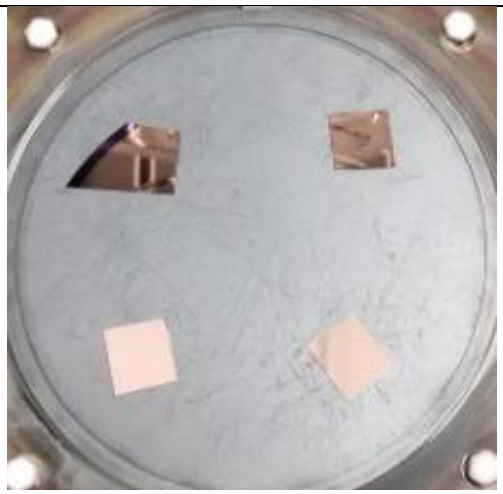

Figure A1: Cu film samples loaded in the Black magic chamber. All samples are loaded 1 cm apart from the stage edge, which usually gives the best quality of graphene on cleaved samples.

A.2. CHEMICAL VAPOR DEPOSITION GRAPHENE ON CU-FOIL TRANSFER

Step	Details
1	Chemical vapor deposition of graphene on Cu foil
2	Attaching Graphene/Cu foil on bare glass carrier (200 μm-thick) using tape to prevent PMMA from permeation between Cu and glass carrier.
3	Spin-coating PMMA A4 on Graphene/Cu/glass carrier with 3000 rpm for 60 sec
4	Bake at 90 ºC for 5 mins
5	Detaching PMMA/Graphene/Cu from the glass carrier
6	Etching Graphene at back-side of Cu foil with oxygen plasma RIE for 1 min (RF power : 50 W, Pressure : 80 mTorr, O_2 flow : 18 sccm)
7	Floating PMMA/Graphene/Cu foil on ammonia persulfate (APS-100) in order to etch Cu foil for overnight
8	Transferring PMMA/Graphene stacks to clean water using a stainless-steel spoon
9	Rinsing (more than 5 times) with clean water
10	Transferring PMMA/Graphene stack to the target substrate
11	Dehydrating the sample for 30 mins and keep the sample in N_2 box overnight to remove residual water
12	Baking at 180 ºC for 2 mins
13	Removing PMMA supporting layer to expose graphene to the air Or Using PMMA for e-beam patterning

A.3. CHEMICAL VAPOR DEPOSITION GRAPHENE ON CU-FILM TRANSFER

Step	Details
1	Chemical vapor deposition of graphene on Cu film/SiO_2/Si
2	Spin-coating PMMA A4 on Graphene/Cu/glass carrier with 3000 rpm for 60 sec
3	Bake at 90 ºC for 5 mins
4	Removing PMMA residues at sidewall of PMMA/Graphene/Cu film/SiO_2/Si sample
5	Etching SiO_2 with BOE to detach PMMA/Graphene/Cu film from Si substrate
6	Transferring (floating) PMMA/Graphene/Cu film to ammonia persulfate (APS-100) in order to etch Cu film for 3 hours* using a stainless-steel spoon *3 hours for 1 µm-thick Cu film
7	Transferring PMMA/Graphene stacks to clean water using a stainless-steel spoon
8	Rinsing (more than 5 times) with clean water
9	Transferring PMMA/Graphene stack to the target substrate
10	Dehydrating the sample for 30 mins and keep the sample in N_2 box overnight to remove residual water
11	Baking at 180 ºC for 2 mins
12	Removing PMMA supporting layer to expose graphene to the air Or Using PMMA for e-beam patterning

A.4. CHEMICAL VAPOR DEPOSITION MoS_2 TRANSFER

Step	Details
1	Chemical vapor deposition of MoS_2 on SiO_2/Si
2	Spin-coating PMMA A4 on MoS_2 on SiO_2/Si with 2000 rpm for 60 sec
3	Baking at 180 ºC for 2 mins
4	Spin-coating PMMA C4 on PMMA A4/MoS_2/SiO_2/Si with 2000 rpm for 60 sec
5	Baking at 180 ºC for 2 mins
6	Removing PMMA residues at sidewall of PMMA/ MoS_2/SiO_2/Si sample
7	Attaching a PDMS layer on PMMA coated substrate
8	Etching SiO_2 with BOE to detach PDMS/PMMA/ MoS_2 from Si substrate
9	Transferring PDMS/PMMA/ MoS_2 stacks to clean water using a stainless-steel spoon
10	Rinsing (more than 5 times) with clean water
11	Transferring PDMS/PMMA/ MoS_2 stack to the target substrate
12	Dehydrating the sample for 30 mins and keep the sample in N_2 box overnight to remove residual water
13	Baking at 180 ºC for 2 mins
14	Removing PMMA middle layer to expose MoS_2 to the air as well as to remove PDMS supporting layer

A.5. PREPARATION OF PAPER SUBSTRATE

Step	Details
1	Preparing commercially available glossy paper (HP), Kapton tape, bare Si carrier wafer
2	Attaching glossy paper to Si wafer with Kapton tape
3	Spin-coating liquid polyimide (PI2574, HD microsystems) with 2000 rpm for 60 sec
4	Baking at 100 ºC for 1 min
5	Curing the sample under vacuum in Whip pro200 oven. The curing process is described below. 1. Temperature ramp rate from RT to 200 ºC : 4 ºC/min 2. Pre-cure at 200 ºC for 30 mins 3. Temperature ramp rate from 200 ºC to 230 ºC : 2 ºC/min 4. Cure at 230 ºC for 50 mins 5. Temperature naturally decreases from 230 ºC to RT as heater is turned off

A.6. PRECISE ALIGNMENT OF JEOL E-BEAM LITHOGRAPHY

The JEOL e-beam lithography tool allows users to pattern nanoscale features (See A.7.) as well as to prevent mask steps from misalignment. First of all, understanding of the principle that how the e-beam system recognizes specific locations on samples is important. In JEOL e-beam system, the principle is that the detector detects reflected e-beam from a metal line in order to get information of the metal's location. RAITH SEM E-beam system, on the other hand, allows users to monitor alignment marks location by SEM, and users input the location information to the e-beam system. Thus, for low misalignment margin processes such as radio frequency transistors, JEOL EBL tool is strongly recommended.

JEOL EBL system has two types of alignment marks (AM); Global AM and Chip AM.

The global AM is composed of 4 plus-shaped metals (so called P, Q, R and S). P and Q (R and S) marks are located in positive x-axis and negative x-axis (positive y-axis and negative y-axis), respectively. These 4 global marks are used to find center of P, Q, R and S marks on samples. The alignment mark thickness should be thicker than 40 nm of Au for sharp reflected e-beam for the detector.

The Chip AMs are composed of 3 "+" shaped metal line, and it can be made when the global AM is patterned and metallized. Note that 3 Chip AM should be in 80 μm by 80 μm that is the field size of e-beam. The Chip AMs are used to correct sample's tilted angle that can happen during sample loading.

A.7. CVD Graphene Radio Frequency Field-Effect Transistor with Six Fingers Layout

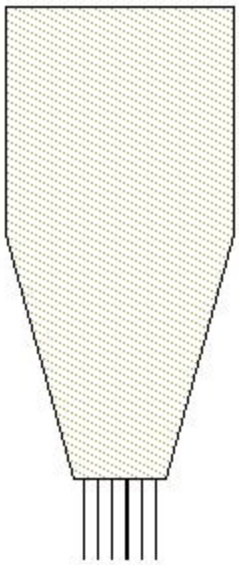

Figure A2: Mask1 for Embedded gate with six fingers and pad.

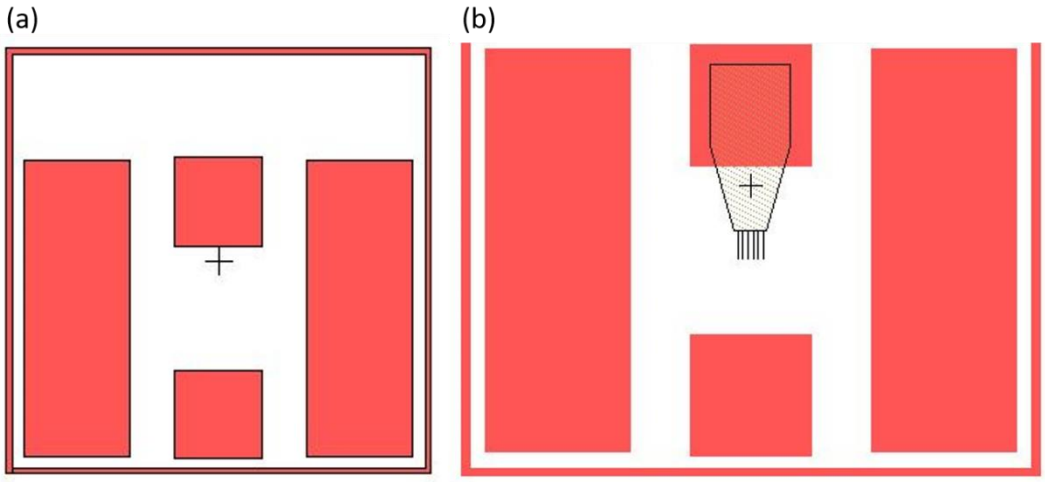

Figure A3: (a) Mask 2 for via pattern. (b) accumulated layout.

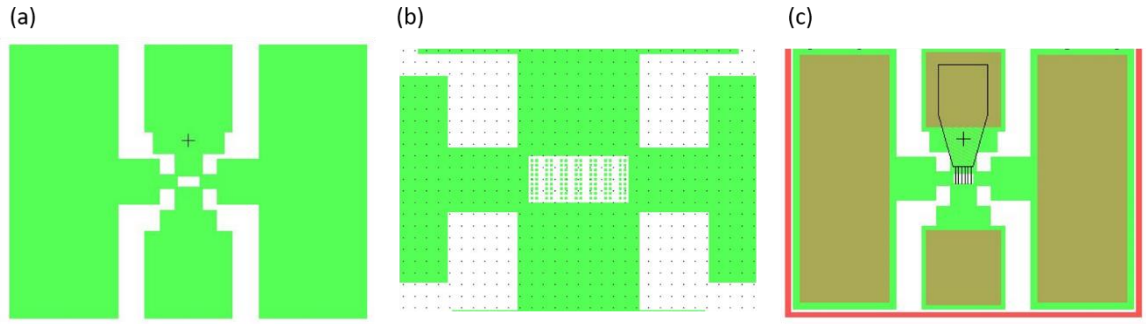

Figure A4: (a) Mask 3 for active channel define. (b) array patterns for contact resistance engineering. (c) accumulated layout.

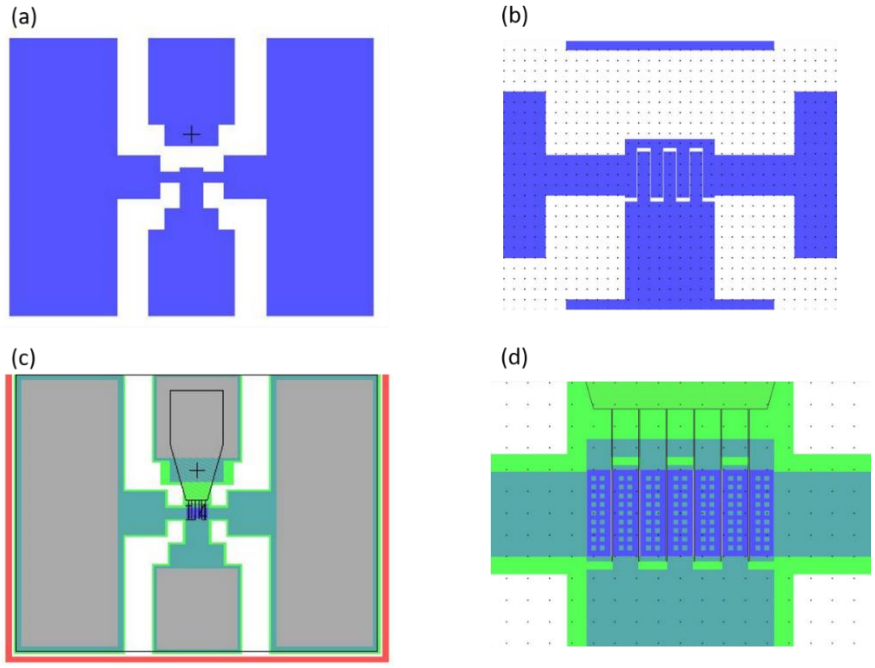

Figure A5: (a) Mask 4 for source and drain. (b) magnified mask 4 layout. (c) accumulated layout. (d) magnified and accumulated all masks

A.8. CVD MoS_2 Radio Frequency Field-Effect Transistor with Dual Fingers Layout

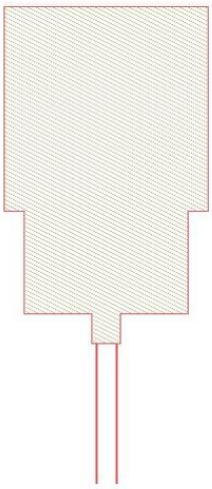

Figure A6: Mask 1 for Embedded gate finger and pad.

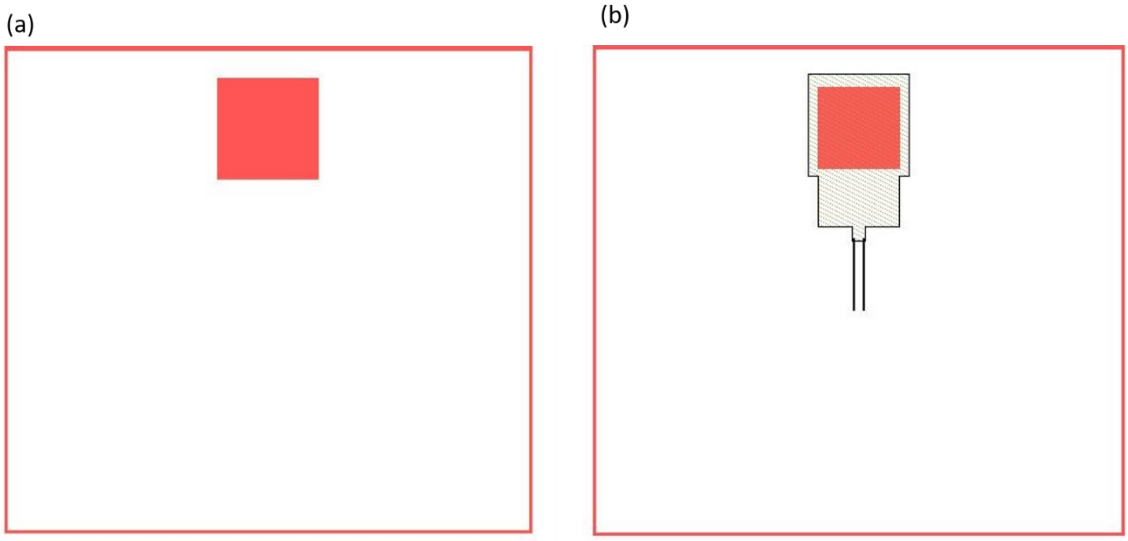

Figure A7: (a) Mask 2 for via pattern. (b) accumulated layout.

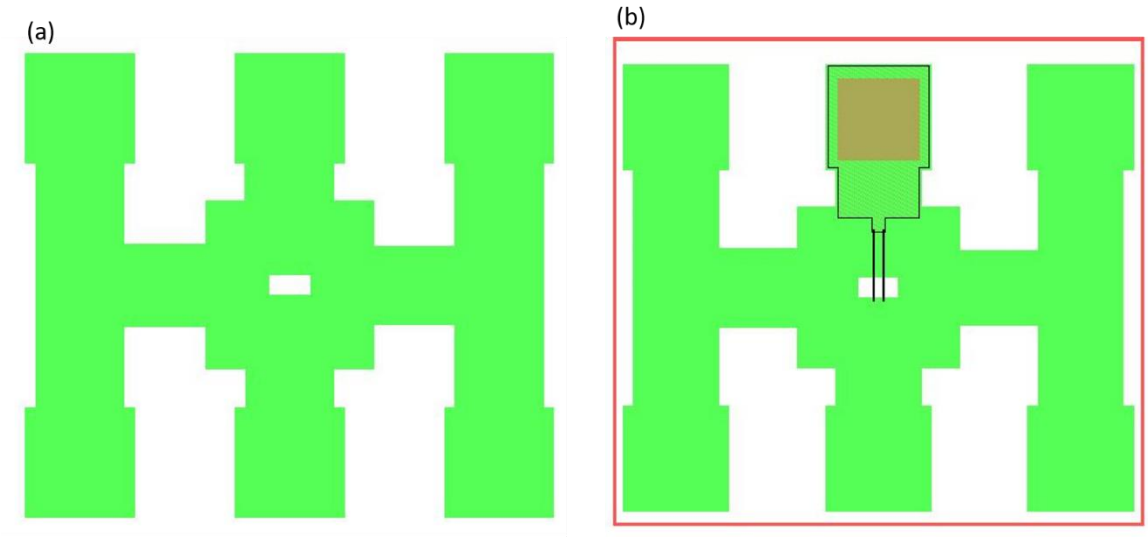

Figure A8: (a) Mask 3 for active channel define. (b) accumulated layout.

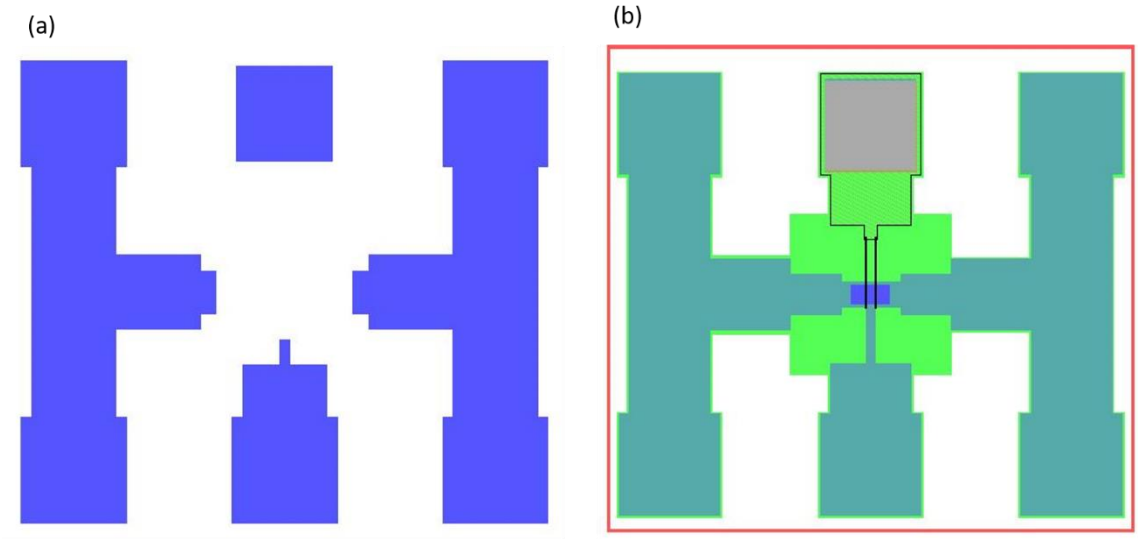

Figure A9: (a) Mask 4 for source and drain. (b) accumulated layout.

A.9. DE-EMBEDDING STRUCTURES

We used OPEN and SHORT structures fabricated on the same device-under-test (DUT) as measured for high frequency parameters. Figure A.9(a) shows an optical image of the OPEN structure. An electron beam lithography (EBL) step exposing the channel region followed by a MoS_2 etch creates an electrical open in the device. Figure A.9(b) shows the SHORT structure. An EBL step across the channel and pad region followed by a metal deposition creates an electrical shorting in gate, source and drain.

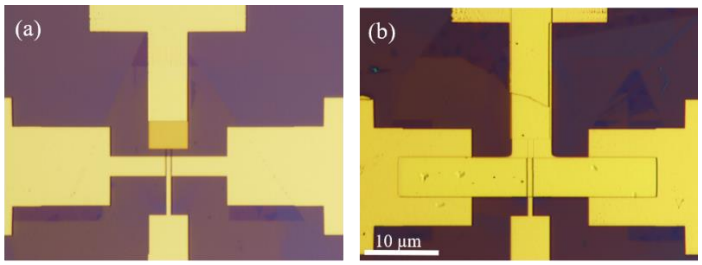

Figure A10: (a) Optical image of the OPEN structure. (d) Optical image of the SHORT structure.

De-embedding on the same DUT provides an accurate removal of parasitic capacitances and inductance characteristic to the measured DUT. The intrinsic RF characteristics are obtained by the following two-step de-embedding processes including OPEN and SHORT. We first obtain S-parameters using VNA, and then using the Agilent ADS simulation tool, the parasitic effects from pads are de-embedded with the following equation.

$$Y_{FET} = ((Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1})^{-1} \qquad \text{(Equation A.9)}$$

References

[1] D. Akinwande, N. Petrone, and J. Hone, "Two-dimensional flexible nanoelectronics," *Nat Commun,* Review vol. 5, pp. 5678, 2014.

[2] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," *Proceedings of the Ieee,* vol. 101, no. 7, pp. 1567-1584, 2013.

[3] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically Thin MoS_2: A New Direct-Gap Semiconductor," *Physical Review Letters,* vol. 105, no. 13, p. 136805, 2010.

[4] A. Molle, J. Goldberger, M. Houssa, Y. Xu, S.-C. Zhang, and D. Akinwande, "Buckled two-dimensional Xene sheets," *Nature Materials,* vol. 16, p. 163, 2017.

[5] W. N. Zhu, M. N. Yogeesh, S. X. Yang, S. H. Aldave, J. S. Kim, S. Sonde, L. Tao, N. S. Lu, and D. Akinwande, "Flexible Black Phosphorus Ambipolar Transistors, Circuits and AM Demodulator," *Nano Letters,* vol. 15, no. 3, pp. 1883-1890, 2015.

[6] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, and D. Akinwande, "Silicene field-effect transistors operating at room temperature," *Nat. Nano,* Letter vol. 10, no. 3, pp. 227-231, 2015.

[7] T. Natsuki and J. Natsuki, "Prediction of mechanical properties for hexagonal boron nitride nanosheets using molecular mechanics model," *Applied Physics A,* vol. 123, no. 4, p. 283, 2017.

[8] A. Loi, I. Manunza, and A. Bonfiglio, "Flexible, organic, ion-sensitive field-effect transistor," *Applied Physics Letters,* vol. 86, no. 10, 2005.

[9] Y. Noguchi, T. Sekitani, and T. Someya, "Organic-transistor-based flexible pressure sensors using ink-jet-printed electrodes and gate dielectric layers," *Applied Physics Letters,* vol. 89, no. 25, p. 3, Dec 2006.

[10] H. T. Yi, M. M. Payne, J. E. Anthony, and V. Podzorov, "Ultra-flexible solution-processed organic field-effect transistors," *Nature Communications,* vol. 3, 2012.

[11] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Communications,* vol. 146, no. 9, pp. 351-355, 2008.

[12] Z. H. Ni, T. Yu, Y. H. Lu, Y. Y. Wang, Y. P. Feng, and Z. X. Shen, "Uniaxial Strain on Graphene: Raman Spectroscopy Study and Band-Gap Opening," *ACS Nano,* vol. 2, no. 11, pp. 2301-2305, 2008.

[13] C. Si, Z. Sun, and F. Liu, "Strain engineering of graphene: a review," *Nanoscale,* vol. 8, no. 6, pp. 3207-3217, 2016.

[14] S. Rahimi, L. Tao, S. F. Chowdhury, S. Park, A. Jouvray, S. Buttress, N. Rupesinghe, K. Teo, and D. Akinwande, "Toward 300 mm Wafer-Scalable High-Performance Polycrystalline Chemical Vapor Deposited Graphene Transistors," *ACS Nano,* vol. 8, no. 10, pp. 10471-10479, 2014.

[15] R. Cheng, S. Jiang, Y. Chen, Y. Liu, N. Weiss, H.-C. Cheng, H. Wu, Y. Huang, and X. Duan, "Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics," *Nature Communications,* vol. 5, p. 5143, 2014.

[16] S. Bertolazzi, J. Brivio, and A. Kis, "Stretching and Breaking of Ultrathin MoS_2," *ACS Nano,* vol. 5, no. 12, pp. 9703-9709, 2011.
[17] B. Radisavljevic, A. Radenovic, B. J, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nat. Nano,* vol. 6, no. 3, pp. 147-150, 2011.
[18] H. Y. Chang, S. X. Yang, J. H. Lee, L. Tao, W. S. Hwang, D. Jena, N. S. Lu, and D. Akinwande, "High-Performance, Highly Bendable MoS_2 Transistors with High-K Dielectrics for Flexible Low-Power Systems," *ACS Nano,* vol. 7, no. 6, pp. 5446-5452, 2013.
[19] H.-Y. Chang, M. N. Yogeesh, R. Ghosh, A. Rai, A. Sanne, S. Yang, N. Lu, S. K. Banerjee, and D. Akinwande, "Large-Area Monolayer MoS_2 for Flexible Low-Power RF Nanoelectronics in the GHz Regime," *Advanced Materials,* vol. 28, no. 9, pp. 1818-1823, 2016.
[20] I. B. Amara, E. B. Salem, and S. Jaziri, "Optoelectronic response and excitonic properties of monolayer MoS_2," *Journal of Applied Physics,* vol. 120, no. 5, p. 051707, 2016.
[21] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance Killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance," *2009 Intenational Electron Devices Meeting (IEDM),* pp. 23.2.1-23.2.4, 2009.
[22] K. N. Parrish and D. Akinwande, "Impact of contact resistance on the transconductance and linearity of graphene transistors (vol 98, 183505, 2011)," *Applied Physics Letters,* vol. 99, no. 23, 2011.
[23] A. Allain, J. Kang, K. Banerjee, and A. Kis, "Electrical contacts to two-dimensional semiconductors," *Nature Materials, Review Article,* vol. 14, p. 1195, 2015.
[24] A. Sanne, S. Park, R. Ghosh, M. N. Yogeesh, C. Liu, L. Mathew, R. Rao, D. Akinwande, and S. K. Banerjee, "Embedded gate CVD MoS_2 microwave FETs," *npj 2D Materials and Applications,* vol. 1, no. 1, p. 26, 2017.
[25] J. Lee, L. Tao, Y. Hao, R. S. Ruoff, and D. Akinwande, "Embedded-gate graphene transistors for high-mobility detachable flexible nanoelectronics," *Applied Physics Letters,* vol. 100, no. 15, p. 152104, 2012.
[26] J. Lee, T. J. Ha, H. Li, K. N. Parrish, M. Holt, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "25 GHz embedded-gate graphene transistors with high-k dielectrics on extremely flexible plastic sheets," *ACS Nano,* vol. 7, no. 9, pp. 7744-50, 2013.
[27] S. Park, W. Zhu, H. Y. Chang, M. N. Yogeesh, R. Ghosh, S. K. Banerjee, and D. Akinwande, "High-frequency prospects of 2D nanomaterials for flexible nanoelectronics from baseband to sub-THz devices," *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 32.1.1-32.1.4, 2015.

[28] S. Park, S. H. Shin, M. N. Yogeesh, A. L. Lee, S. Rahimi, and D. Akinwande, "Extremely High-Frequency Flexible Graphene Thin-Film Transistors," *IEEE Electron Device Letters,* vol. 37, no. 4, pp. 512-515, 2016.

[29] C. Kim, I. Moon, D. Lee, M. S. Choi, F. Ahmed, S. Nam, Y. Cho, H.-J. Shin, S. Park, and W. J. Yoo, "Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides," *ACS Nano,* vol. 11, no. 2, pp. 1588-1596, 2017.

[30] S. Rumyantsev, G. Liu, M. S. Shur, R. A. Potyrailo, and A. A. Balandin, "Selective gas sensing with a single pristine graphene transistor," *Nano Lett,* vol. 12, no. 5, pp. 2294-8, 2012.

[31] J. Lee, K. N. Parrish, S. F. Chowdhury, T. J. Ha, Y. F. Hao, L. Tao, A. Dodabalapur, R. S. Ruoff, D. Akinwande, and Ieee, "State-of-the-art Graphene Transistors on Hexagonal Boron Nitride, High-k, and Polymeric Films for GHz Flexible Analog Nanoelectronics," *2012 IEEE International Electron Devices Meeting (IEDM),* pp. 4, 2012.

[32] J. Lee, L. Tao, K. N. Parrish, Y. F. Hao, R. S. Ruoff, D. Akinwande, and Ieee, "Highly Bendable High-mobility Graphene Field Effect Transistors with Multi-finger Embedded Gates on Flexible Substrates," *2012 12th Ieee Conference on Nanotechnology (Ieee-Nano),* pp. 3, 2012.

[33] G. H. Lee, Y. J. Yu, X. Cui, N. Petrone, C. H. Lee, M. S. Choi, D. Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, "Flexible and Transparent MoS_2 Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures," *ACS Nano,* vol. 7, no. 9, pp. 7931-7936, 2013.

[34] S. Das, R. Gulotty, A. V. Sumant, and A. Roelofs, "All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor," *Nano Letters,* vol. 14, no. 5, pp. 2861-2866, 2014.

[35] M. E. Ramon, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Three-Gigahertz Graphene Frequency Doubler on Quartz Operating Beyond the Transit Frequency," *IEEE Transactions on Nanotechnology,* vol. 11, no. 5, pp. 877-883, 2012.

[36] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. W. Wang, R. G. Gordon, M. Lundstrom, and H. J. Dai, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-k gate dielectrics," *Nano Letters,* vol. 4, no. 3, pp. 447-450, 2004.

[37] Y. G. Seol, H. Y. Noh, S. S. Lee, J. H. Ahn, and N. E. Lee, "Mechanically flexible low-leakage multilayer gate dielectrics for flexible organic thin film transistors," *Applied Physics Letters,* vol. 93, no. 1, p. 3, 2008.

[38] S.-H. Jen, J. A. Bertrand, and S. M. George, "Critical tensile and compressive strains for cracking of Al_2O_3 films grown by atomic layer deposition," *Journal of Applied Physics,* vol. 109, no. 8, 2011.

[39] J. Liu, D. B. Buchholz, R. P. H. Chang, A. Facchetti, and T. J. Marks, "High-Performance Flexible Transparent Thin-Film Transistors Using a Hybrid Gate Dielectric and an Amorphous Zinc Indium Tin Oxide Channel," *Advanced Materials,* vol. 22, no. 21, pp. 2333-2337, 2010.

[40] H. Ohuchi, Y. Takayanagi, H. Yano, Z. F. Duan, T. Okukawa, Y. Yanagi, A. Yoshida, and Y. Nishioka, "Flexible Transistors with Low Temperature Curable Polyimide Gate Insulator," *Journal of Photopolymer Science and Technology,* vol. 25, no. 3, pp. 381-383, 2012.

[41] H. T. Yi, Y. Chen, K. Czelen, and V. Podzorov, "Vacuum Lamination Approach to Fabrication of High-Performance Single-Crystal Organic Field-Effect Transistors," *Advanced Materials,* vol. 23, no. 48, pp. 5807, 2011.

[42] Y. Kato, S. Iba, R. Teramoto, T. Sekitani, T. Someya, H. Kawaguchi, and T. Sakurai, "High mobility of pentacene field-effect transistors with polyimide gate dielectric layers," *Applied Physics Letters,* vol. 84, no. 19, pp. 3789-3791, 2004.

[43] S. Park, H.-Y. Chang, S. Rahimi, A. Lee, and D. Akinwande, "Flexible 2D electronics using nanoscale transparent polyimide gate dielectric," *2015 73rd Annual Device Research Conference (DRC),* pp. 193-194, 2015.

[44] S. Park, H.-Y. Chang, S. Rahimi, A. L. Lee, L. Tao and D. Akinwande, "Transparent Nanoscale Polyimide Gate Dielectric for Highly Flexible Electronics," *Advanced Electronic Materials*, vol. 4, no. 2, pp. 1700043, 2018.

[45] J. Pu, Y. Yomogida, K.-K. Liu, L.-J. Li, Y. Iwasa, and T. Takenobu, "Highly Flexible MoS_2 Thin-Film Transistors with Ion Gel Dielectrics," *Nano Letters,* vol. 12, no. 8, pp. 4013-4017, 2012.

[46] B. Fallahazad, K. Lee, G. Lian, S. Kim, C. M. Corbet, D. A. Ferrer, L. Colombo, and E. Tutuc, "Scaling of Al_2O_3 dielectric for graphene field-effect transistors," *Applied Physics Letters,* vol. 100, no. 9, pp. 4, 2012.

[47] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, "Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates," *Thin Solid Films,* vol. 413, no. 1–2, pp. 186-197, 2002.

[48] H. C. Lin, P. D. Ye, and G. D. Wilk, "Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al_2O_3 on GaAs," *Applied Physics Letters,* vol. 87, no. 18, pp. 182904, 2005.

[49] X. Yu, L. Zeng, N. Zhou, P. Guo, F. Shi, D. B. Buchholz, Q. Ma, J. Yu, V. P. Dravid, R. P. H. Chang, M. Bedzyk, T. J. Marks, A. Facchetti, "Ultra-Flexible, “Invisible” Thin-Film Transistors Enabled by Amorphous Metal Oxide.Polymer Channel Layer Blends," *Advanced Materials*, vol. 27, no. 14, pp. 2390-2399, 2015.

[50] J. Y. Kim, J. Lee, W. H. Lee, I. N. Kholmanov, J. W. Suk, T. Kim, Y. F. Hao, H. Chou, D. Akinwande, and R. S. Ruoff, "Flexible and Transparent Dielectric Film

with a High Dielectric Constant Using Chemical Vapor Deposition-Grown Graphene Interlayer," *ACS Nano,* vol. 8, no. 1, pp. 269-274, 2014.

[51] R. W. Snyder, B. Thomson, B. Bartges, D. Czerniawski, and P. C. Painter, "FTIR Studies of Polyimides - Thermal Curing," *Macromolecules,* vol. 22, no. 11, pp. 4166-4172, 1989.

[52] H. Y. Chang, W. N. Zhu, and D. Akinwande, "On the mobility and contact resistance evaluation for transistors based on MoS_2 or two-dimensional semiconducting atomic crystals," *Applied Physics Letters,* vol. 104, no. 11, 2014.

[53] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Applied Physics Letters,* vol. 94, no. 6, pp. 3, 2009.

[54] Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science,* vol. 327, no. 5966, pp. 662-662, 2010.

[55] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin, "State-of-the-Art Graphene High-Frequency Electronics," *Nano Letters,* vol. 12, no. 6, pp. 3062-3067, 2012.

[56] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proceedings of the National Academy of Sciences of the United States of America (PNAS),* vol. 109, no. 29, pp. 11588-11592, 2012.

[57] C.-H. Yeh, Y.-W. Lain, Y.-C. Chiu, C.-H. Liao, D. R. Moyano, S. S. H. Hsu, and P.-W. Chiu, "Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits," *ACS Nano,* vol. 8, no. 8, pp. 7663-7670, 2014.

[58] J. Lee, H. Y. Chang, T. J. Ha, R. S. Ruoff, A. Dodabalapur, and D. Akinwande, "High-Performance Flexible Nanoelectronics: 2D Atomic Channel Materials for Low-Power Digital and High-Frequency Analog Devices," *2013 IEEE International Electron Devices Meeting (IEDM)*, pp. 19.2.1–19.2.4, 2013.

[59] A. L. Moore and L. Shi, "Emerging challenges and materials for thermal management of electronics," *Materials Today,* vol. 17, no. 4, pp. 163-174, 2014.

[60] Y. Q. Wu, Y. M. Lin, K. A. Jenkins, J. A. Ott, C. Dimitrakopoulos, D. B. Farmer, F. Xia, A. Grill, D. A. Antoniadis, and P. Avouris, "RF performance of short channel graphene field-effect transistor," *2010 IEEE Electron Devices Meeting (IEDM),* pp. 9.6.1-9.6.3, 2010.

[61] H. K. Gummel, "On definition of cutoff frequency-f_T," *Proceedings of the Ieee,* vol. 57, no. 12, pp. 2159, 1969.

[62] C. Wang, J.-C. Chien, H. Fang, K. Takei, J. Nah, E. Plis, S. Krishna, A. M. Niknejad, and A. Javey, "Self-Aligned, Extremely High Frequency III-V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates," *Nano Letters,* vol. 12, no. 8, pp. 4140-4145, 2012.

[63] W. Zhu, D. B. Farmer, K. A. Jenkins, B. Ek, S. Oida, X. Li, J. Bucchignano, S. Dawes, E. A. Duch, and P. Avouris, "Graphene radio frequency devices on flexible substrate," *Applied Physics Letters,* vol. 102, no. 23, 2013.

[64] Q. Guoxuan, S. Jung-Hun, Z. Yang, Z. Han, Z. Weidong, W. Yuxin, M. Jianguo, and M. Zhenqiang, "RF Characterization of Gigahertz Flexible Silicon Thin-Film Transistor on Plastic Substrates Under Bending Conditions," *Electron Device Letters, IEEE,* vol. 34, no. 2, pp. 262-264, 2013.

[65] K. N. Parrish and D. Akinwande, "Impact of contact resistance on the transconductance and linearity of graphene transistors," *Applied Physics Letters,* vol. 98, no. 18, pp. 3, 2011.

[66] V. E. Dorgan, M.-H. Bae, and E. Pop, "Mobility and saturation velocity in graphene on SiO_2," *Applied Physics Letters,* vol. 97, no. 8, 2010.

[67] X. Li, J. T. Mullen, Z. Jin, K. M. Borysenko, M. Buongiorno Nardelli, and K. W. Kim, "Intrinsic electrical transport properties of monolayer silicene and MoS_2 from first principles," *Physical Review B,* vol. 87, no. 11, pp. 115418, 2013.

[68] D. Krasnozhon, D. Lembke, C. Nyffeler, Y. Leblebici, and A. Kis, "MoS_2 Transistors Operating at Gigahertz Frequencies," *Nano Letters,* vol. 14, no. 10, pp. 5905-5911, 2014.

[69] D. Krasnozhon, S. Dutta, C. Nyffeler, Y. Leblebici, and A. Kis, "High-frequency, scaled MoS_2 transistors," *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 27.4.1-27.4.4, 2015.

[70] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande, and S. Banerjee, "Radio Frequency Transistors and Circuits Based on CVD MoS_2," *Nano Letters,* vol. 15, no. 8, pp. 5039-5045, 2015.

[71] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, and K. A. Jenkins, "Current Saturation in Submicrometer Graphene Transistors with Thin Gate Dielectric: Experiment, Simulation, and Theory," *ACS Nano,* vol. 6, no. 6, pp. 5220-5226, 2012.

[72] L. Yu, D. El-Damak, S. Ha, X. Ling, Y. Lin, A. Zubair, Y. Zhang, Y. H. Lee, J. Kong, A. Chandrakasan, and T. Palacios, "Enhancement-mode single-layer CVD MoS_2 FET technology for digital electronics," in *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 32.3.1-32.3.4, 2015.

[73] H. J. Conley, B. Wang, J. I. Ziegler, R. F. Haglund, S. T. Pantelides, and K. I. Bolotin, "Bandgap Engineering of Strained Monolayer and Bilayer MoS_2," *Nano Letters,* vol. 13, no. 8, pp. 3626-3630, 2013.

[74] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, "Field-Effect Transistors Built from All Two-Dimensional Material Components," *ACS Nano,* vol. 8, no. 6, pp. 6259-6264, 2014.

[75] A. Rai, A. Valsaraj, H. C. P. Movva, A. Roy, E. Tutuc, L. F. Register, and S. K. Banerjee, "Interfacial-oxygen-vacancy mediated doping of MoS_2 by high-k

dielectrics," *2015 73rd Annual Device Research Conference (DRC)*, pp. 189-190, 2015.

[76] A. Sanne, R. Ghosh, A. Rai, H. C. P. Movva, A. Sharma, R. Rao, L. Mathew, and S. K. Banerjee, "Top-gated chemical vapor deposited MoS_2 field-effect transistors on Si3N4 substrates," *Applied Physics Letters,* vol. 106, no. 6, 2015.

[77] A. Rai, A. Valsaraj, H. C. P. Movva, A. Roy, R. Ghosh, S. Sonde, S. Kang, J. Chang, T. Trivedi, R. Dey, S. Guchhait, S. Larentis, L. F. Register, E. Tutuc, and S. K. Banerjee, "Air Stable Doping and Intrinsic Mobility Enhancement in Monolayer Molybdenum Disulfide by Amorphous Titanium Suboxide Encapsulation," *Nano Letters,* vol. 15, no. 7, pp. 4329-4336, 2015.

[78] K. Kang, S. Xie, L. Huang, Y. Han, P. Y. Huang, K. F. Mak, C.-J. Kim, D. Muller, and J. Park, "High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity," *Nature,* Letter vol. 520, no. 7549, pp. 656-660, 2015.

[79] B. Peng, X. Ren, Z. Wang, X. Wang, R. C. Roberts, and P. K. L. Chan, "High performance organic transistor active-matrix driver developed on paper substrate," *Scientific Reports,* vol. 4, p. 6430, 2014.

[80] K. Yong-Hoon, M. Dae-Gyu, and H. Jeong-In, "Organic TFT array on a paper substrate," *IEEE Electron Device Letters,* vol. 25, no. 10, pp. 702-704, 2004.

[81] C. Qian, J. Sun, J. Yang, and Y. Gao, "Flexible organic field-effect transistors on biodegradable cellulose paper with efficient reusable ion gel dielectrics," *RSC Advances,* vol. 5, no. 19, pp. 14567-14574, 2015.

[82] Y. H. Jung, T.-H. Chang, H. Zhang, C. Yao, Q. Zheng, V. W. Yang, H. Mi, M. Kim, S. J. Cho, D.-W. Park, H. Jiang, J. Lee, Y. Qiu, W. Zhou, Z. Cai, S. Gong, and Z. Ma, "High-performance green flexible electronics based on biodegradable cellulose nanofibril paper," *Nature Communications,* vol. 6, p. 7170, 2015.

[83] S. Park and D. Akinwande, "First Demonstration of High Performance 2D Monolayer Transistors on Paper Substrates," *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 5.2.1-5.2.4, 2017